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CONTRACT NAS9-9334

SOLID STATE SEQUENCER SYSTEM

PHASE II

SUMMARY REPORT

MARCH 1971

Prepared for

NATIONAL AERONAUTICS AND SPACE ADMINISTRATION
MANNED SPACECRAFT CENTER
HOUSTON, TEXAS 77058

MARTIN MARIETTA CORPORATION
P.O. Box 179
Denver, Colorado 80201

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Approved By

David E. Leck

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Program Manager

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TABLE OF CONTENTS

APPENDICES

1. SYSTEM OPERATION

1.1 Application of Power

When the sequencer is connected to the test tool, the test tool power shall be turned on before applying power to the sequencer. The TEST-OPERATE switch on the test tool must be in the OPERATE position before applying power to the sequencer. Power to the test tool consists of 115V, 60 Hz to power the tape reader and + 5Vdc ± 0.2Vdc to power the logic circuits. The 5V supply must be capable of supplying 5 amperes. Because the output circuits are magnetically isolated from the logic circuits and cannot turn on without a direct command from the logic circuits, the LOGIC BUS and the PYRO BUS may be turned on and off in any order. When LOGIC BUS power is applied to the sequencer, it will automatically recycle and read the last command word from the memory that occurred before power was turned off. In most instances, this will be a STOP command and the STOP light on the test tool will turn on indicating that this has been done. At the same time the ADDRESS REGISTER lights on the test tool should indicate the address immediately following the STOP command.

1.2 Loading

To load a program into the S-4 system, the proper cables from the test tool must be plugged into J9 and J10. Next, the tape is inserted into the tape reader. With the POWER switch ON, turning the FEED switch up will cause the tape to run through the reader. The tape should be started and stopped in the section where only feed holes occur. One cycle of the tape is sufficient to load the sequencer. To stop the tape, turn the FEED switch down.

Connector, J10, is used only for loading and to provide timing pulses for the ADDRESS REGISTER display. To minimize the possibility of noise affecting the sequencer, this connector may be removed and the shorting plug inserted. This should only be done with LOGIC BUS POWER OFF.

1.3 Sequencing

Once a program has been loaded, it can be initiated by turning the PROGRAM START switch up. In the case of the operational program, this sets up the initial conditions such that the sequencer is monitoring for either LIFTOFF or ON PAD ABORT (TRANSLATION CONTROLLER CCW) events. From this point, the program is controlled by the event inputs.

Reset Conditions - The program and S-4 system are constructed to automatically reset all input events in the following situations:

1. When the program is loaded and initiated.
2. When the program goes through the Earth Landing Sequence - whether this sequence is used on normal reentry or as part of an abort sequence.
3. When the program goes through the Reset Sequence. NOTE: the program only enters the Reset Sequence when LIFTOFF has occurred and when the Reset-Clear Switch on the test tool is pushed up to the Reset condition. This switch exists on the test tool for checkout purposes and will not be present in a spacecraft.
4. When the Reset-Clear switch is pushed down to the CLEAR position (this clears the memory address register) and the INITIATE switch is then pushed up.

WARNING!

WHENEVER ANY OF THE ABOVE SITUATIONS HAS OCCURRED, THE OX DUMP ENABLE SWITCH AND THE AUTO ABORT SWITCH MUST BE TURNED OFF AND THEN ON BEFORE PROCEEDING FURTHER WITH SYSTEM OPERATION.

2. SYSTEM DESCRIPTION

2.1 General

The Solid State Sequencer System (S4) is a highly reliable stored program type system that is designed to control several independent sequences. It consists of a master unit located in the Command Module hereafter referred to as the CMU and the Service Module Jettison Controller located in the Service Module and hereafter referred to as the SMU. A block diagram of the CMU is shown in Figure 2-1. The system is controlled via input events and provides time delays by the count down of a basic crystal controlled clock. Sequential programing is used with the time interval stored being defined as the time between an event and an output or time between two outputs. Ground isolation of outputs permits power busses to be separated as required for a particular application. Programs are loaded into the system via paper tape. Sequence position is maintained despite power dropouts of any duration. Time counts in progress are recycled for power dropouts greater than 0.5 sec. Provision is made for disabling the 0.5 sec dropout function as desired.

2.2 Performance

2.2.1 Temperature Range - The CMU is designed to operate over a temperature range from $0^{\circ}F$ to $160^{\circ}F$. However, components have been selected so that operation could be extended from $-30^{\circ}F$ to $+190^{\circ}F$ if required. The SMU has been designed to operate from $-25^{\circ}F$ to $+200^{\circ}F$.

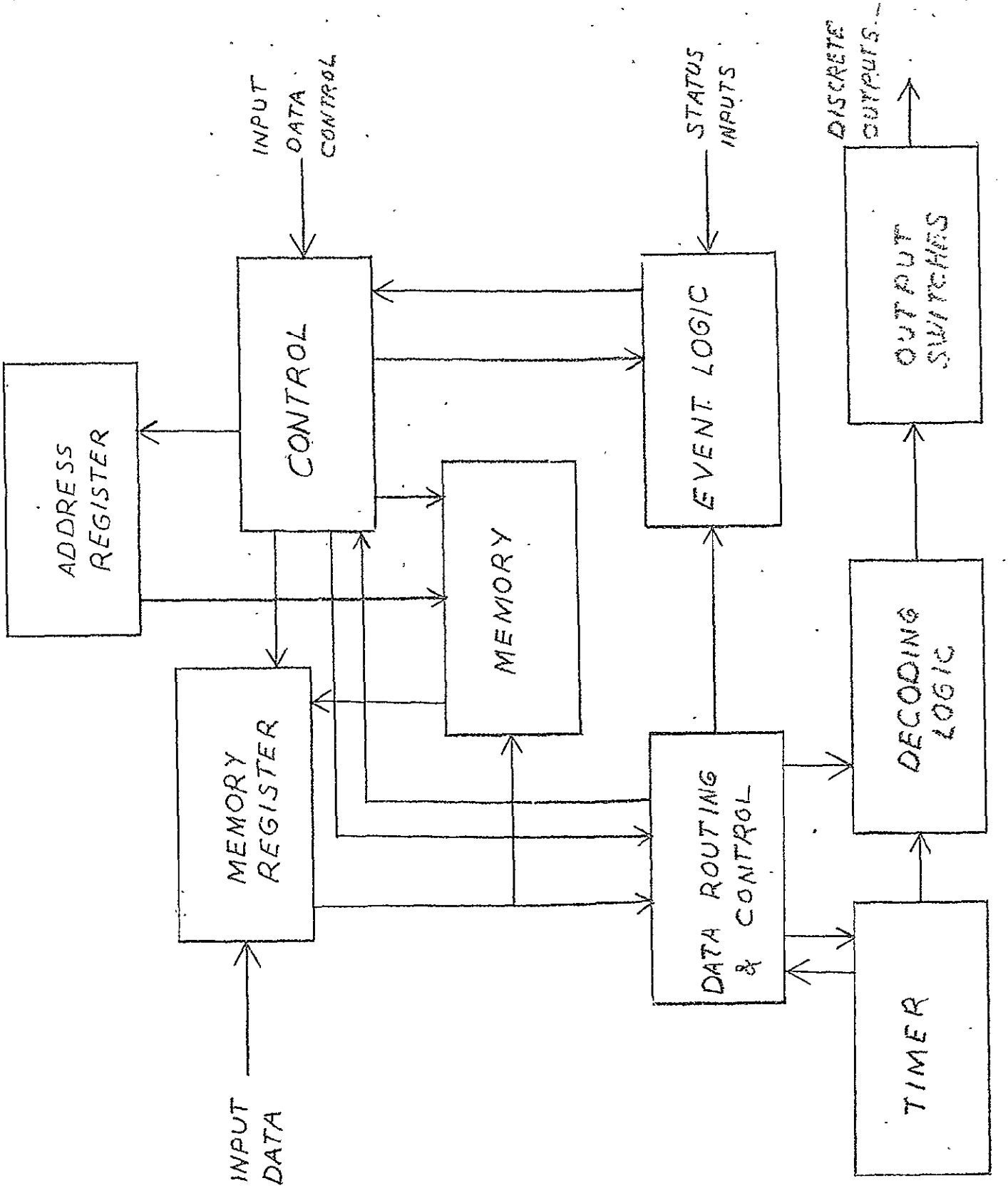
2.2.2 Timing

An 8 MHz crystal controlled oscillator is used as the basic clock from which all system timing is derived. Four clock frequencies (10 KHz, 1 KHz, 100 Hz, and 10 Hz) are provided for sequence timing. These frequencies are counted down in a twelve-stage binary counter providing a time interval selection from 100 microseconds to 409.6 seconds. The count is accurate to within 1 pulse of the 10 KHz clock $\pm$ an oscillator error of .01% over the temperature range. When selecting time intervals of less than 100 milliseconds, the program delay should also be taken into account. This program delay will be constant to the tolerance of the crystal clock. The reasons for program delay will be explained in Section 4.3 Program Construction.

2.2.3 Event Logic

To provide sequence control, two event logic blocks are provided. The inputs to these event blocks may be generated either from switches controlled by the astronaut (EDS ABORT ENABLE), or from external events (LIFTOFF) or from sequence controlled outputs ($T > 42$ sec). The two event logic blocks (ELB's) operate independently with ELB #2 having priority over ELB #1. The use of the two ELB's permits two different event combinations to be monitored at one time.

FIGURE 2-1


INPUT DATA CONTROL
STATUS INPUTS
DISCRETE OUTPUTS
CONTROL
EVENT LOGIC
OUTPUT SWITCHES
ADDRESS REGISTER
MEMORY
MEMORY REGISTER
DATA ROUTING & CONTROL
DECODING LOGIC
TIMER
INPUT DATA

Allowance has been made in the program for up to 17 event inputs per ELB. Howeve to minimize package size, thirteen (13) inputs for ELB #1 and eight (8) inputs for ELB #2 have been implemented. This includes 2 spares in ELB #1 and 1 spare in ELB #2. Each ELB can be programed to look for an OR combination of any number of its input events, or for an AND combination of two or three events, or for an N-1 or N-2 out of N combination where N can be any number of specific events from two to fourteen.

When an event equation has been satisfied, a branching operation is initiated. This provides the capability of branching to a particular sequence or of conditional branching within a sequence.

The event logic may be used in an "immediate" mode or in a monitor mode. In the immediate mode, an equation is loaded into the event logic and a YES or NO answer is obtained If the answer is YES, a branch operation is initiated. If the answer is NO, the event logic is cleared and the program continues in sequence. In the monitor mode, if the answer is NO, the event logic is not cleared but continues to monitor for the specified set of event conditions.

2.2.4 Decoding and Output Switches

A magnetic core decoder, using current steering techniques, has been chosen to drive the output switches. The reasons for this are: minimum power consumption; isolation of output switch grounds; high noise immunity; and memory capability. The last attribute provides a capability for turning back on those output switches which may have been turned off as a result of a power interruption.

All output switches have been designed for zero power dissipation while in the OFF condition. The pulse output from the magnetic decoder is used to turn on latching switches which, in turn, drive the high power output stages. Two types of latching circuits are used; those that are automatically reset when a self-contained timer times out; and those that are reset via a separate command from the decoder.

2.3 Program Construction

The S4 has a ferrite core memory with a capacity of 1024 words by 12 bits per word. Because of reliability considerations, only 512 words with 11 bits per word are available for the program. Two types of system words are stored in the memory; timing words and event words. Each timing word uses two memory words, while each event word uses three memory words. The bit allocation for these words is shown in Table 1. Table 2 gives the command designation and output switches associated with each output function. Table 3 gives the number assigned to each input event.

FOLDOUT FRAME

MARTIN MARIETTA CORPORATION
DENVER DIVISION

BY JRY DATE 7-22-69 SUBJECT BIT DESIGNATION

CHKD. BY ..... DATE .....

TABLE I

	BIT NR-	TIMING
MEMORY READ #1 WORD	0	FUNCTION CODE
	1	CLOCK CODE . 0 10
	2	CLOCK CODE 0.
	3	TIMING BIT 0 (L
	4	TIMING BIT 1
	5	TIMING BIT 2
	6	TIMING BIT 3
	7	TIMING BIT 4
	8	TIMING BIT 5
	9	TIMING BIT 6
	10	TIMING BIT 7
	11	PARITY
MEMORY READ #2 WORD	0	TIMING BIT 8
	1	TIMING BIT 9
	2	TIMING BIT 10
	3	TIMING BIT 11
	4	ALWAYS 0
	5	COMMAND BIT
	6	COMMAND BIT
	7	COMMAND BIT
	8	COMMAND BIT
	9	COMMAND BIT
	10	COMMAND BIT
	11	PARITY
MEMORY READ #3 WORD	0	
	1	
	2	
	3	
	4	
	5	
	6	
	7	
	8	
	9	
	10	
	11	

FOLDOUT FRAME 2

SHEET NO.....OF.....
JOB NO. NAS9-933X
ISSUE A

WORD	EVENT WORD	
FOR TIMING WORD	FUNCTION CODE 1 FOR EVENT WORD	0
1 1KHz 0 100 Hz 1 10Hz	BLOCK SELECTOR CODE 0-BLK 1 1-BLK 2	1
0 1 1	ALWAYS 0	2
B)	CHECK TIME CODE 0-IMMEDIATE 1-MONITOR	3
	SET INHIBIT #1	4
	SET INHIBIT #2	5
	BRANCH ADDRESS 0 (LSB)	6
	BRANCH ADDRESS 1	7
	BRANCH ADDRESS 2	8
	BRANCH ADDRESS 3	9
	BRANCH ADDRESS 4	10
	PARITY	11
	BRANCH ADDRESS 5	0
	BRANCH ADDRESS 6	1
	BRANCH ADDRESS 7	2
	BRANCH ADDRESS 8	3
	BRANCH ADDRESS 9 (ALWAYS 0)	4
(MSB)	EVENT SET 1	5
	EVENT SET 2	6
	EVENT SET 3	7
	EVENT SET 4	8
	EVENT SET 5	9
	EVENT SET 6	10
	PARITY	11
	EVENT SET 7	0
	EVENT SET 8	1
	EVENT SET 9	2
	EVENT SET 10	3
	EVENT SET 11	4
	EVENT SET 12	5
	EVENT SET 13	6
	EVENT SET 14	7
	EVENT SET 15	8
	EVENT SET 16	9
	EVENT SET 17	10
	PARITY	

TABLE 2

COMMAND IMPLEMENTATION CHART

OUTPUT FUNCTIO	CMND NO. OCTAL	MATRIX LOAD	TYPE OUTPUT CIRCUIT	LOAD	REMARKS
T>42 SECONDS	71	125MS LATCH 1 & 2	- - -	- - -	EVENT LOGIC INPUT
INITIATE SM JETTISON	73	125MS LATCH 5 & 6	- - -		TO SMJC
SEPARATE LM-SLA	40	S/R LATCH 25 & 26	PAC 1 & 2	PFC 1 & 2	RESET BY COMMAND NO. 27
SEPARATE LM-SLA	42	PFC 1 & 2		4 PYROS	
REMOVE POWER FROM LM TENSION TIE PYROS	27				RESET S/R LATCH 25 & 26
CUT LM-LV UMBILICAL	44	PFC 3		1 PYRO	
BECO RESET EVENT TIMER	04 04	S/R LATCH 5 & 6	BECO CKT 100 MA SW. 1	200 Ω EVENT TIMER	RESET BY COMMAND NO. 61
BECO OFF	61				RESET S/R LATCH 5 & 6
CM-SM ELECTRICAL-PWR TRANSFER	53	125 MS LATCH 9 & 10	MSD 1	2 MOTOR SWITCHES	
LES ABORT ENABLE	02	S/R LATCH 7 & 8	100 MA SW 2	ABORT INDICATOR	RESET BY COMMAND NO. 57
RESET ABORT INDICATION	57		-		RESET S/R LATCH 7 & 8
CM-SM DEADFACE	22	PFC 4 & 5		4 PYROS	
DUMP OXIDIZER	10	PFC 6 & 7		3 PYROS	
CLOSE OX ISOLATION VALVES	54	S/R LATCH 9 & 10	SD1	2 SOLENOIDS	RESET BY COMMAND NO. 62
OX ISOL. VALVE CMND OFF	62				RESET S/R LATCH 9 & 10
CM-SM RCS TRANSFER	07	125 MS LATCH 15 & 16	MSD 2	2 MOTOR SWITCHES	
CM-SM SEP. ACCOMPLISHED	07			G & N INPUT	
PRESSURIZE CM RCS	36	PFC 8		2 PYROS	
CM-SM SEPARATION	30	S/R LATCH 27 & 28	PAC 5 & 6	PFC 9 & 10	RESET BY COMMAND NO. 25
CM-SM SEPARATION	32	PFC 9 & 10		4 PYROS	
CM-SM SEP. PYRO CUTOFF	25				RESET S/R LATCH 27 & 28
LES MOTOR IGNITE	12	PFC 11		1 PYRO	
PITCH CONTROL MOTOR IGNITE	13	PFC 12		1 PYRO	
ENABLE CM RCS	05	S/R LATCH 11 & 12	0.5A SW 1		RESET BY COMMAND NO. 64
INHIBIT CM RCS	64				RESET S/R LATCH 11 & 12
FUEL DUMP	14	PFC 13 & 14		3 PYROS	
CLOSE FUEL ISOLATION VALVES	55	S/R LATCH 13 & 14	SD 2	2 SOLENOIDS	RESET BY COMMAND NO. 63
FUEL ISOL. VALVE CMND OFF	63				RESET S/R LATCH 13 & 14
DEPLOY CANARD	16	PFC 15		1 PYRO	
ENERGIZE ELS BUS	01	S/R LATCH 15 & 16	100 MASW 3	24K BAROSW.	RESET BY COMMAND NO. 56
DE-ENERGIZE ELS BUS	56				RESET S/R LATCH 15 & 16
TOWER LEG. FRANG NUTS	11	PFC 16 & 17		4 PYROS	
ET JETTISON MOTOR	17	PFC 18		1 PYRO	
LM DOCKING RING FINAL SEP.	45	PFC 27		1 PYRO	
APEX COVER JETTISON	33	PFC 19		7 PYROS	
POWER TO LANYARD SWITCHES	24	PFC 28		1 PYRO	
DEPLOY DROGUE CHUTE	34	PFC 20		2 PYROS	
CM RCS PURGE	15	PFC 21 & 22		4 PYROS	
ACTIVATE 11K BAROSWITCH	03	S/R LATCH 19 & 20	100 MASW 4		RESET BY COMMAND NO. 60
DE-ACTIVATE 11K BAROSWITCH	60				RESET S/R LATCH 19 & 20
DISCONNECT DROGUE CHUTE	35	PFC 23		2 PYROS	
DEPLOY PILOT CHUTE	23	PFC 24 & 25		3 PYROS	
SM "+X" JETS SPS ABORT ACCOMPLISHED INHIBIT P & Y STABILIZATION	74	S/R LATCH 21 & 22	SD 3 & 4	4 SOLENOIDS G & N INPUT	RESET BY COMMAND NO. 66
SM "+X" JETS OFF	66				RESET S/R LATCH 21 & 22
SEPARATE CSM-SLA	43	PFC 26		1 PYRO	
ENABLE SM RCS	75	S/R LATCH 23 & 24	0.5A SW 2		RESET BY COMMAND 50
INHIBIT SM RCS	50				RESET S/R LATCH 23 & 24
RESET ELS 1	21	CLEAR DRIVER 1 & 2			
RESET ELS 2	26	CLEAR DRIVER 3 & 4			
STOP PROGRAM	31	NONE			LOGIC OUTPUT
GO SIGNAL ON	00	S/R LATCH 31 & 32			RESET BY COMMAND NO. 77
GO SIGNAL OFF	77				RESET S/R LATCH
SPARE	06				
SPARE	20				
SPARE	37				
SPARE	41				
SPARE	46				
SPARE	47				
SPARE	51				
SPARE	52				
SPARE	65				
SPARE	67				
SPARE	72				
SPARE	76				

TABLE 3

EVENT LOGIC INPUT SIGNALS

EVENT LOGIC BLOCK NO. 1

EVENT NO.	EVENT NAME	SIGNAL DESCRIPTION	CTL RESET CONDITIONS
1.	LIFTOFF	Positive for 120 sec.	———
2.	E T OFF	Positive Level	———
3.	EDS AUTO ABORT ENABLE SWITCH IN 'AUTO' POSITION	Positive Level	ZERO LEVEL
4.	EDS ABORT SIGNAL #1	Zero Level	Positive Level
5.	EDS ABORT SIGNAL #2	Zero Level	Positive Level
6.	EDS ABORT SIGNAL #3	Zero Level	Positive Level
7.	SPARE		
8.	T > 42 SEC.	Positive for 0.125 Sec.	
9.	OXIDE DUMP ENABLE	Positive Level	ZERO LEVEL
10.	24K BAROSWITCH CLOSURE	Positive Level	
11.	11K BAROSWITCH CLOSURE	Positive Level	
12.	GO SIGNAL	Positive Level	Zero Level
13.	SPARE		

TABLE 3

EVENT LOGIC INPUT SIGNALS

(Continued)

EVENT LOGIC BLOCK NO. 2

CONDITION	EVENT NO.	EVENT NAME	SIGNAL DESCRIPTION	CTL RESET CONDITIONS
A	1.	TRANSLATION CONTROLLER ROTATED CCW	Positive Level	TRANSLATOR CONTROLLER TO NEUTRAL (See Event No. 2)
$\overline{A}$	2.	TRANSLATION CONTROLLER RETURN TO NEUTRAL	Zero Level	RESET BY EVENT NO. 1.
C	3.	CM-SM SEPARATION INITIATION	Positive Level	RESET BY CM-SM SEP. TO OFF (Zero Level)
B	4.	LM-SLA SEPARATION INITIATION	Positive Level	RESET BY LM-SLA SEP. TO OFF (Zero Level)
E	5.	ELS ENABLE	Positive Level	RESET BY ELS ENABLE TO OFF (Zero Level)
D	6.	TEST	Positive Level	RESET BY TEST SW TO OFF (Positive Level)
F	7.	RESET	Positive Level	
	8.	SPARE		

System operation is such that 30 microseconds is required to read and process a timing word and 70 microseconds is required to read an event word and obtain an answer from the event logic. If the answer from the event logic is YES, an additional 100 microseconds is required to complete the branching operation. These delays along with the time required to turn on switched power must be taken into consideration when programing time delays.

An updated program flow chart is given in Figure 2-2/

2.4 Reliability Considerations

The S4 system has been designed to meet a reliability goal of 0.999999 for two channel operation with the additional requirement that no single failure produces an inadvertent output. To meet the latter requirement, each channel contains two essentially separate paths, both of which must operate properly for an output to be generated. Exceptions to this philosophy occur in two areas: the memory electronics and the 8 MHz oscillator.

Because of the large number of discrete component involved in the memory electronics, a poor reliability number was obtained when using the same reliability approach to the memory area as had been used in the rest of the system. The approach finally used required the use of some extra circuitry, but resulted in functional triple redundancy in the memory electronics, thereby permitting correct functioning despite any single failure. As a result, the memory electronics is the most reliable subsystem in the S4.

The 8 MHz oscillator was designed so that the circuit would operate only at 8 MHz. Component failure will cause the circuit to stop oscillating but cannot cause oscillations at a different frequency. This approach eliminates the need to provide a separate oscillator and the circuitry required to compare them.

Each output switch is series redundant, and both parallel paths of logic within a channel must operate correctly for an output switch to be energized.

2.5 Power Considerations

The S4 has been designed to minimize power consumption. This has been accomplished by using switched power on those portions of the system (such as the memory electronics) which are in use for only a small part of the time that the system is in operation. Those portions of the system that require constant power (such as the clock, timer, and event logic) have been implemented with low power integrated circuits and core-transistor logic (CTL's) to reduce power consumption. The average system

power consumption (for the overall sequencer operating time during a mission) does not vary much from the standby power consumption which is about 8.5 watts.

Switched power is turned on whenever an event equation is satisfied or upon the completion of a timing count. Basically, this involves turning on transistor switches to transfer energy from the storage capacitors in the power supply into filter capacitors located throughout the system. A fixed delay of 400 microseconds has been allowed for this operation. When a system word containing a timing count or a stop command is read from the memory, switched power is turned off. This involves turning off the transistor switches and dumping the switched voltages applied to the memory drive circuits. This operation takes 6 milliseconds. These two time delays must be taken into account when constructing a program although the 6 millisecond delay is usually not critical since most system time delays are of longer duration.

FIGURE 2-2

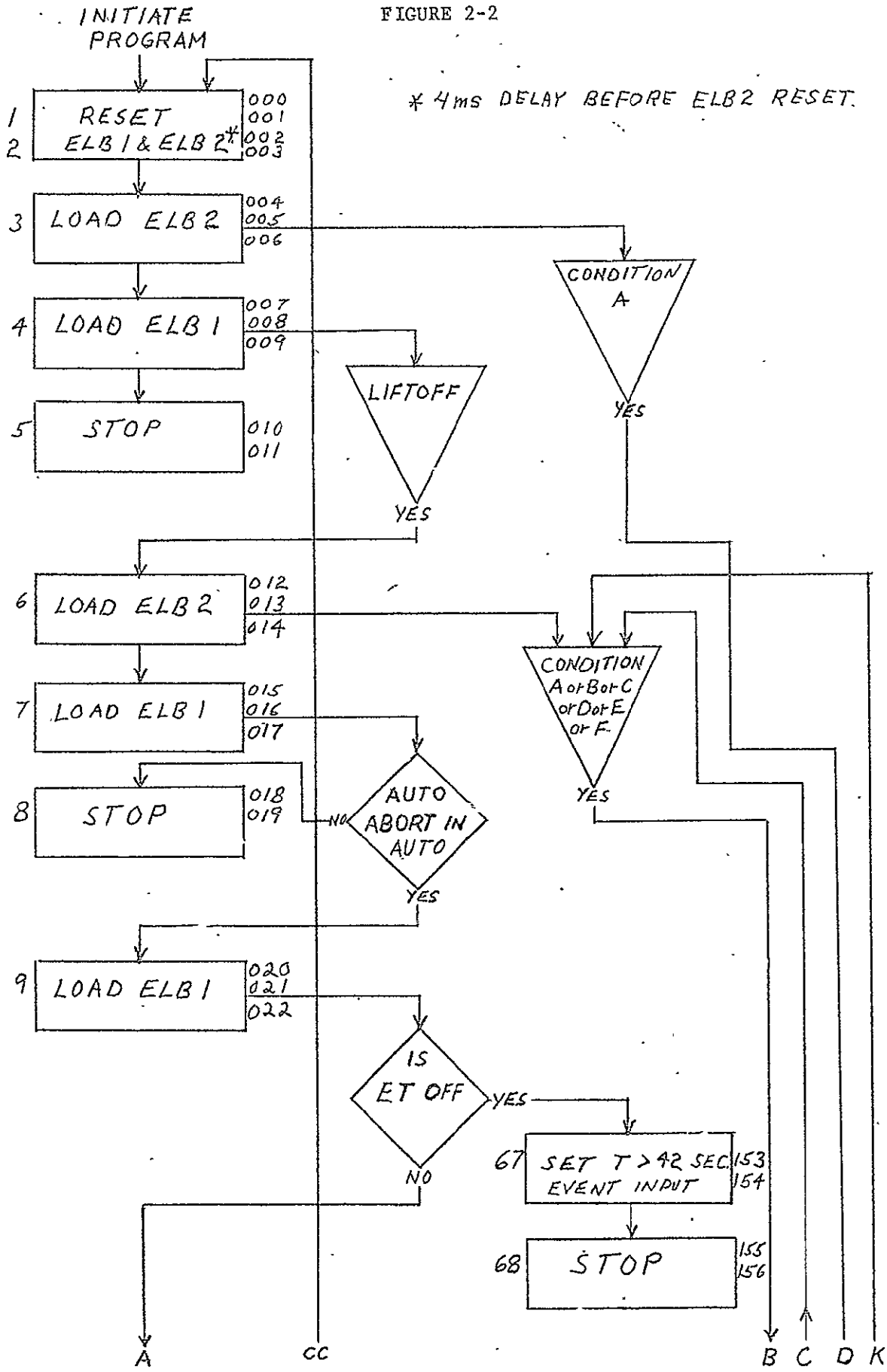
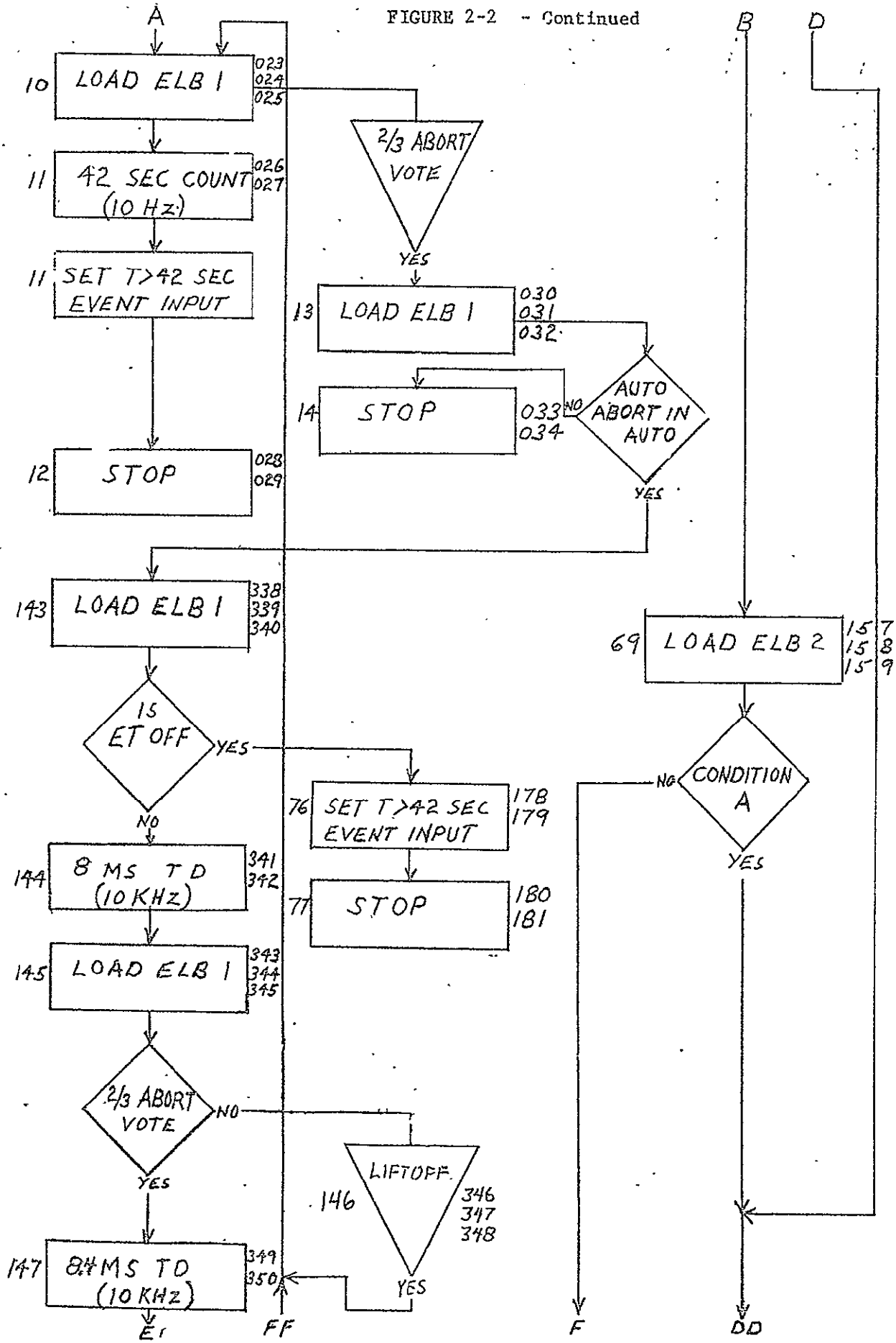

INITIATE PROGRAM
* 4ms DELAY BEFORE ELB2 RESET.
1
2
RESET ELB1 & ELB2*
000
001
002
003
3
LOAD ELB2
004
005
006
4
LOAD ELB1
007
008
009
5
STOP
010
011
LIFTOFF
YES
CONDITION A
YES
6
LOAD ELB2
012
013
014
7
LOAD ELB1
015
016
017
8
STOP
018
019
AUTO ABORT IN AUTO
NO
YES
CONDITION A or B or C or D or E or F
YES
9
LOAD ELB1
020
021
022
IS ET OFF
YES
NO
67
SET T > 42 SEC EVENT INPUT
153
154
68
STOP
155
156
A
CC
B
C
D
K

FIGURE 2-2 - Continued



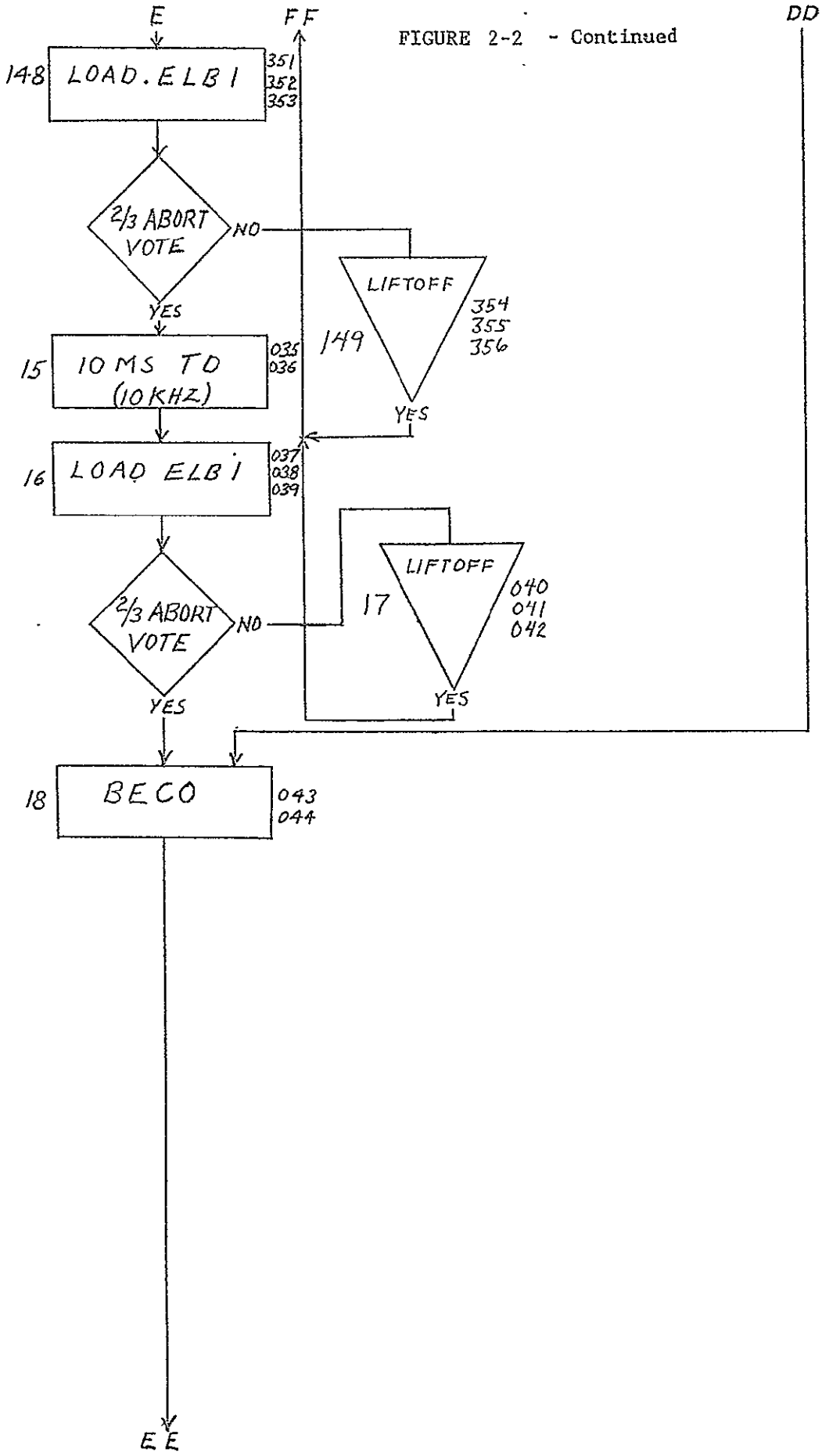


FIGURE 2-2 - Continued

FIGURE 2-2 - Continued

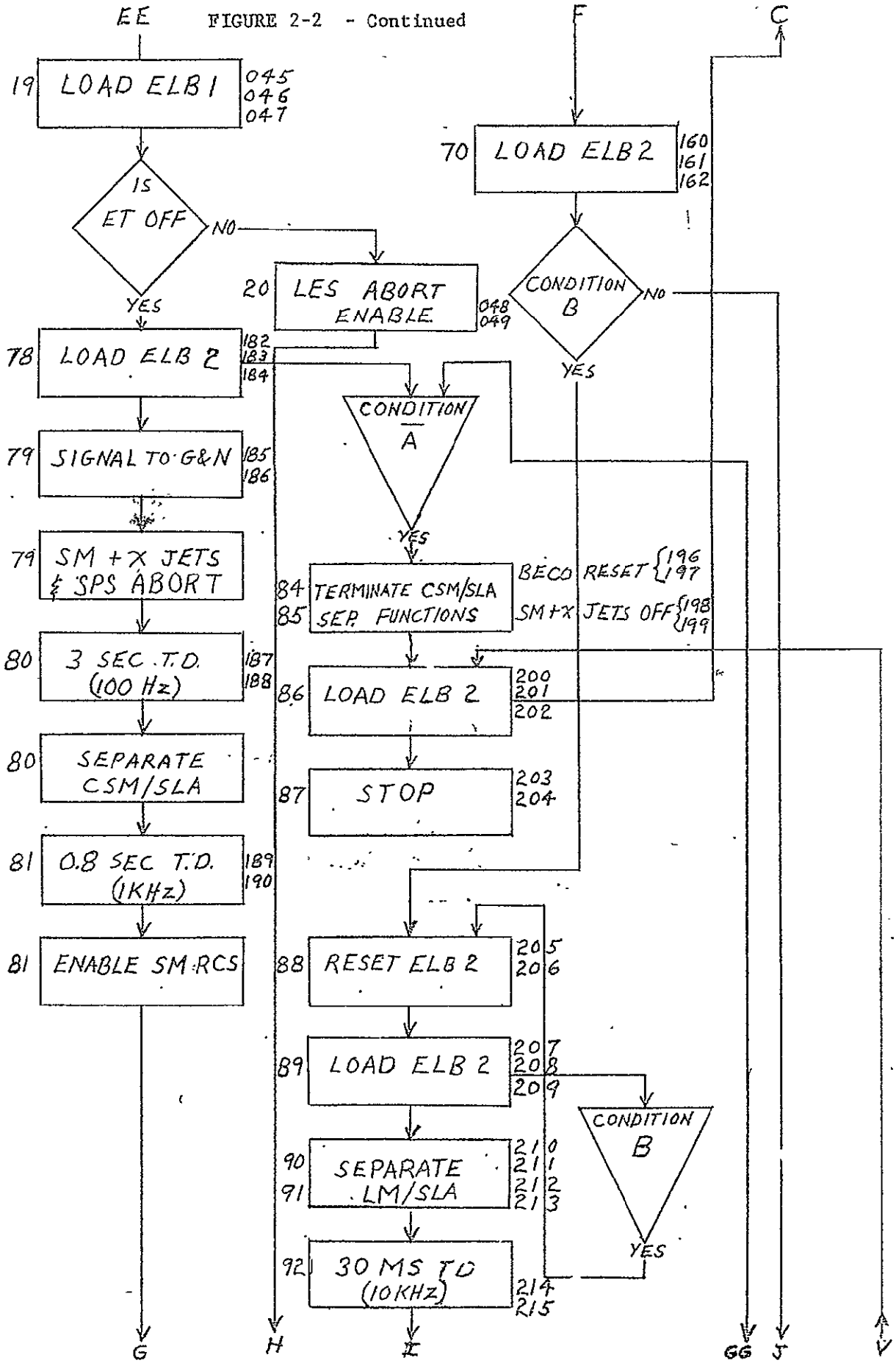


FIGURE 2-2 - Continued

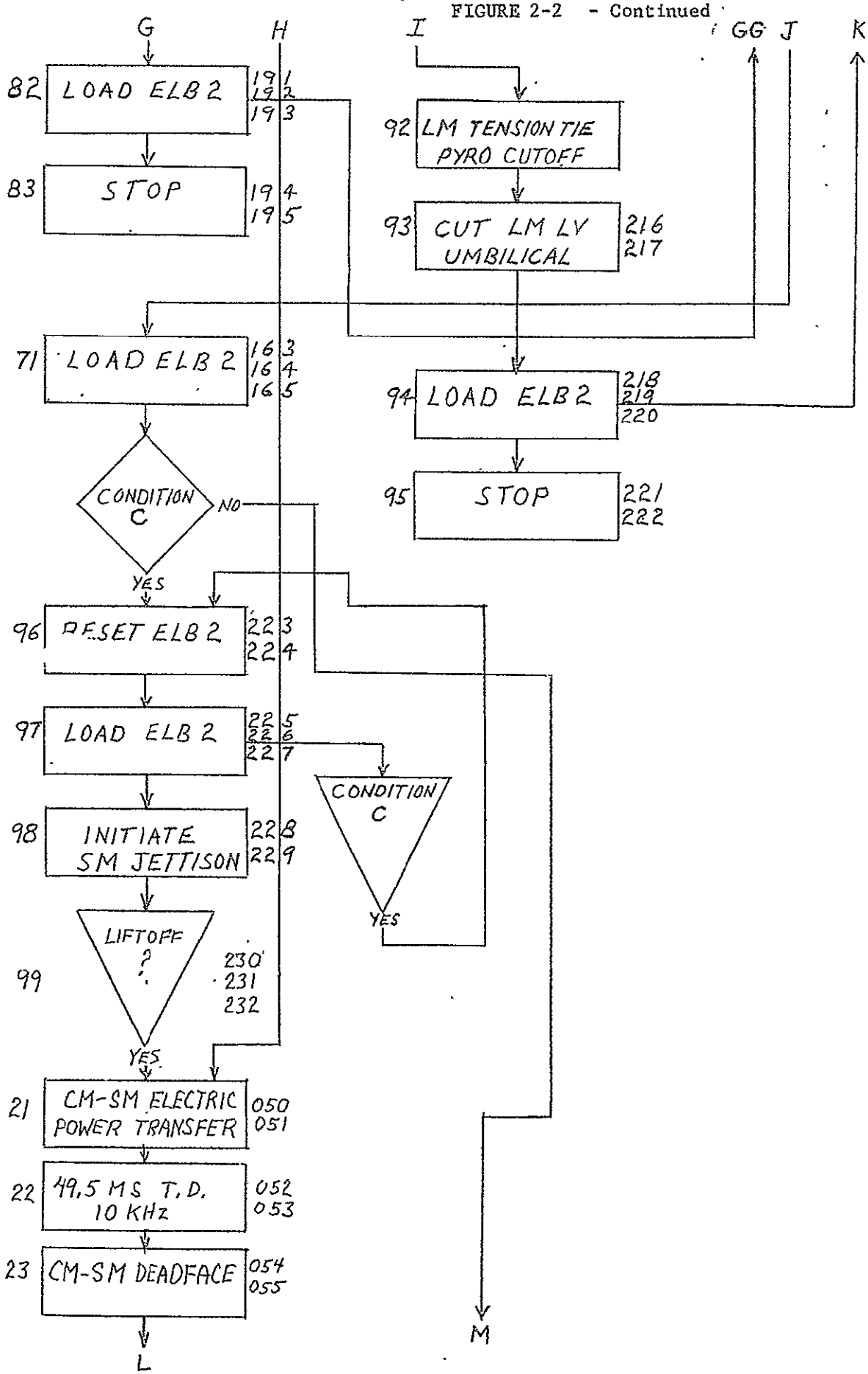
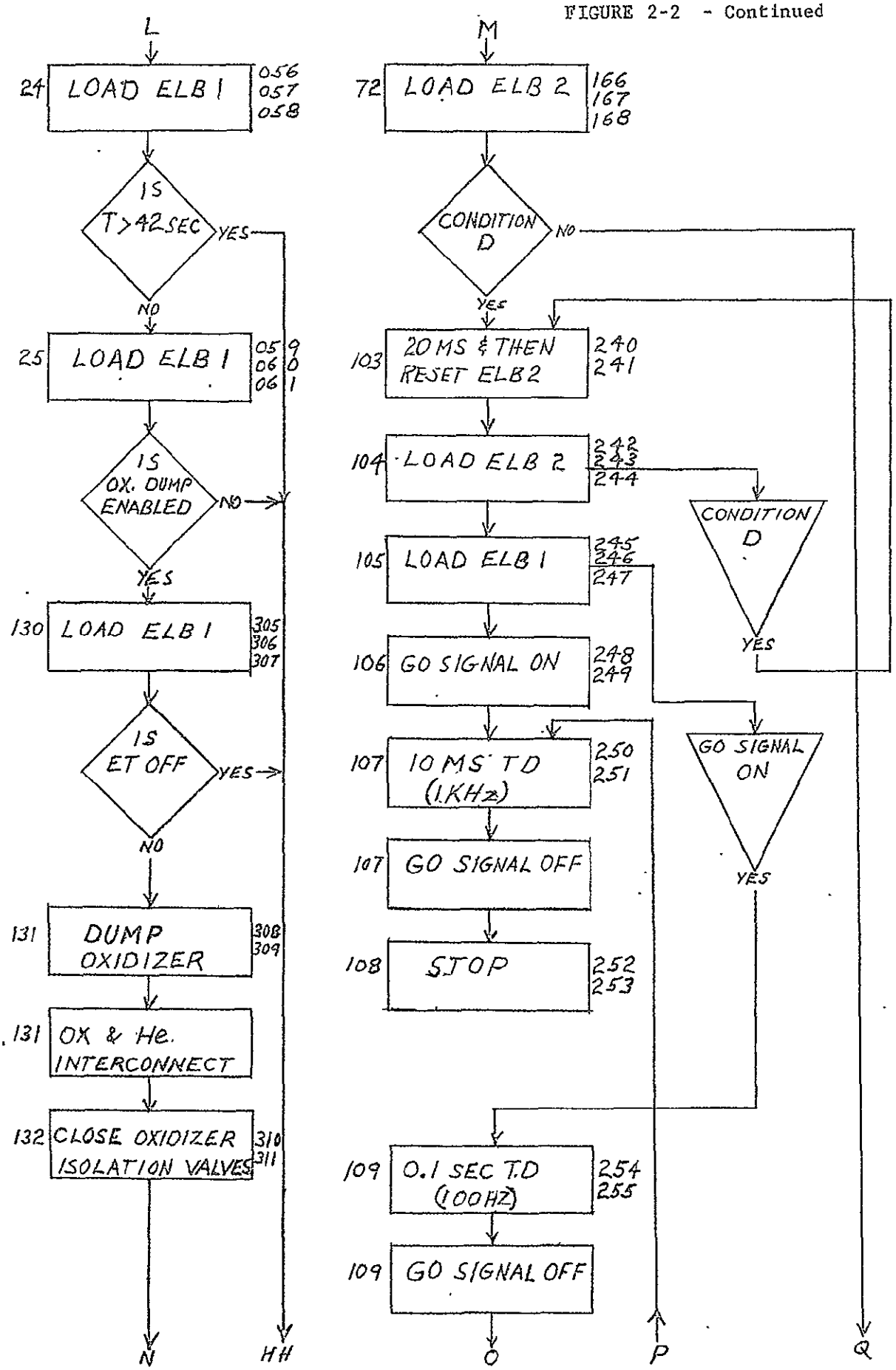


FIGURE 2-2 - Continued



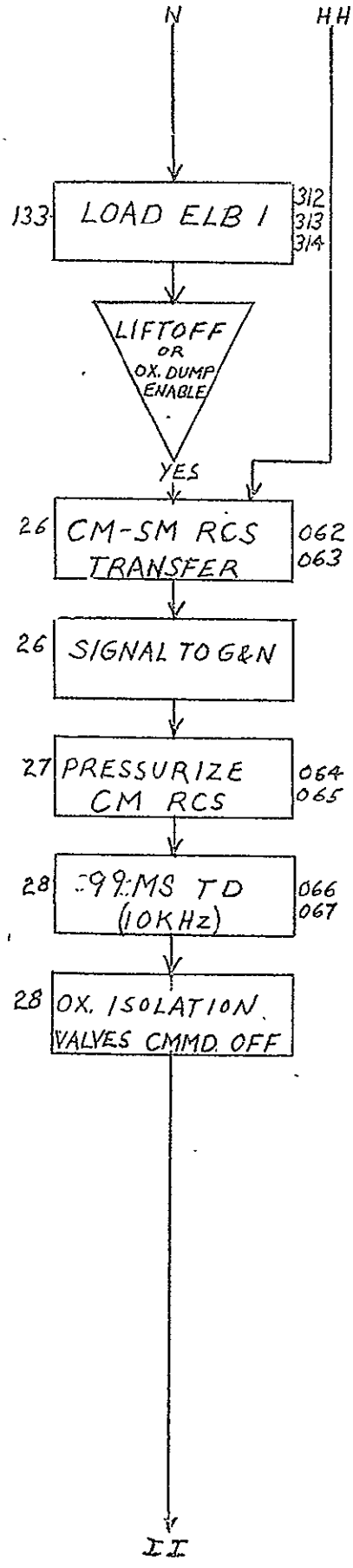


FIGURE 2-2 - Continued

FIGURE 2-2 - Continued

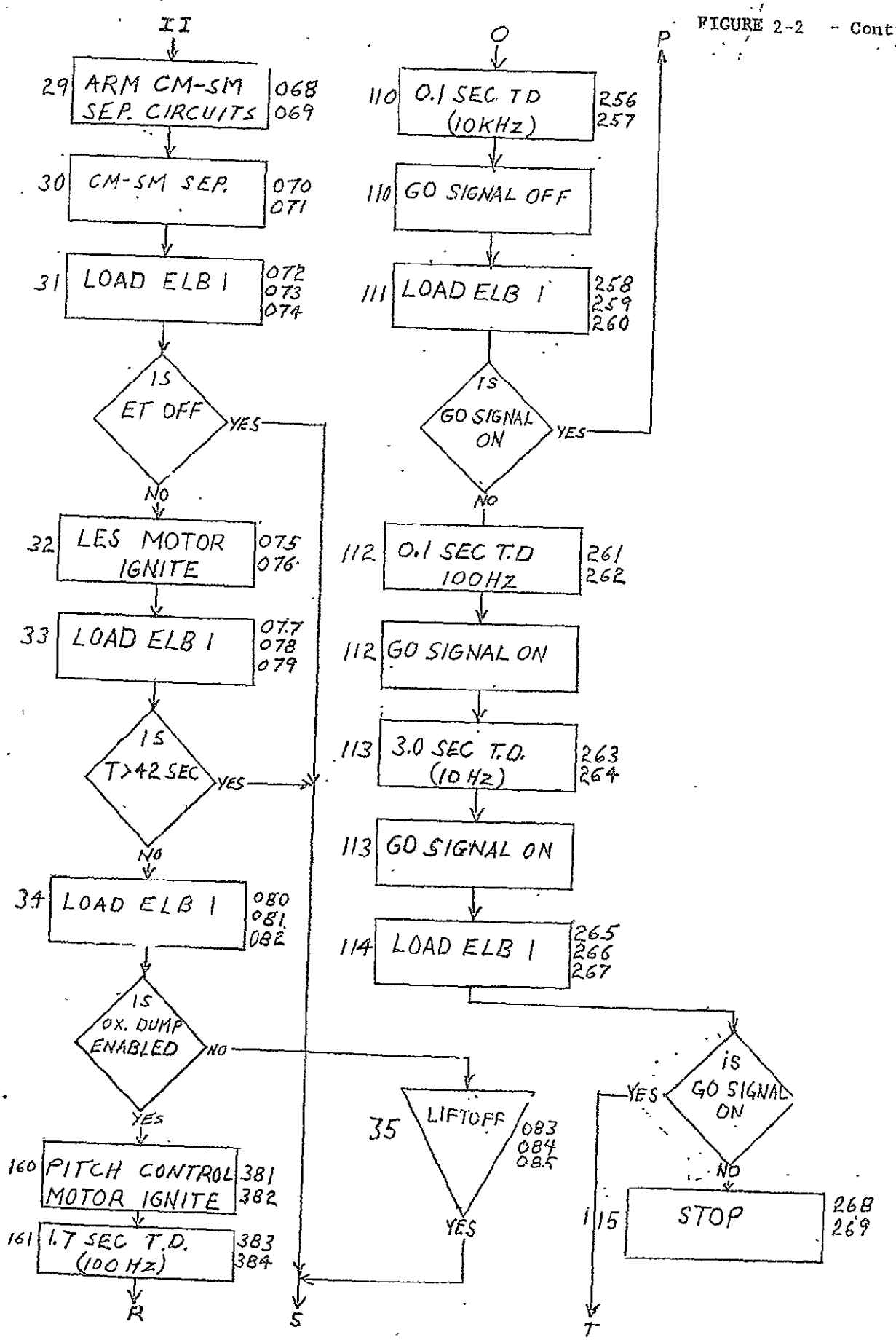
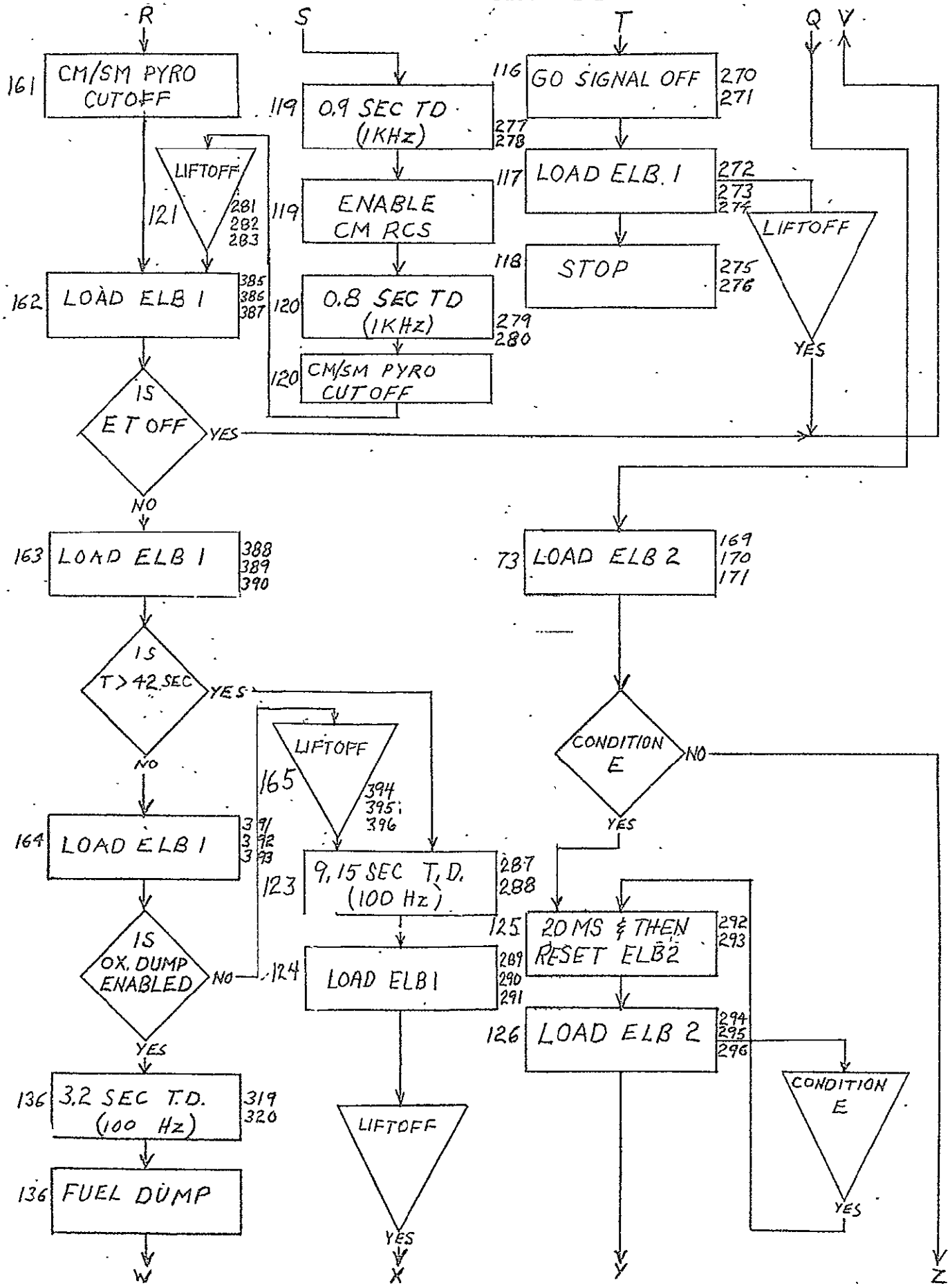


FIGURE 2-2. - Continued



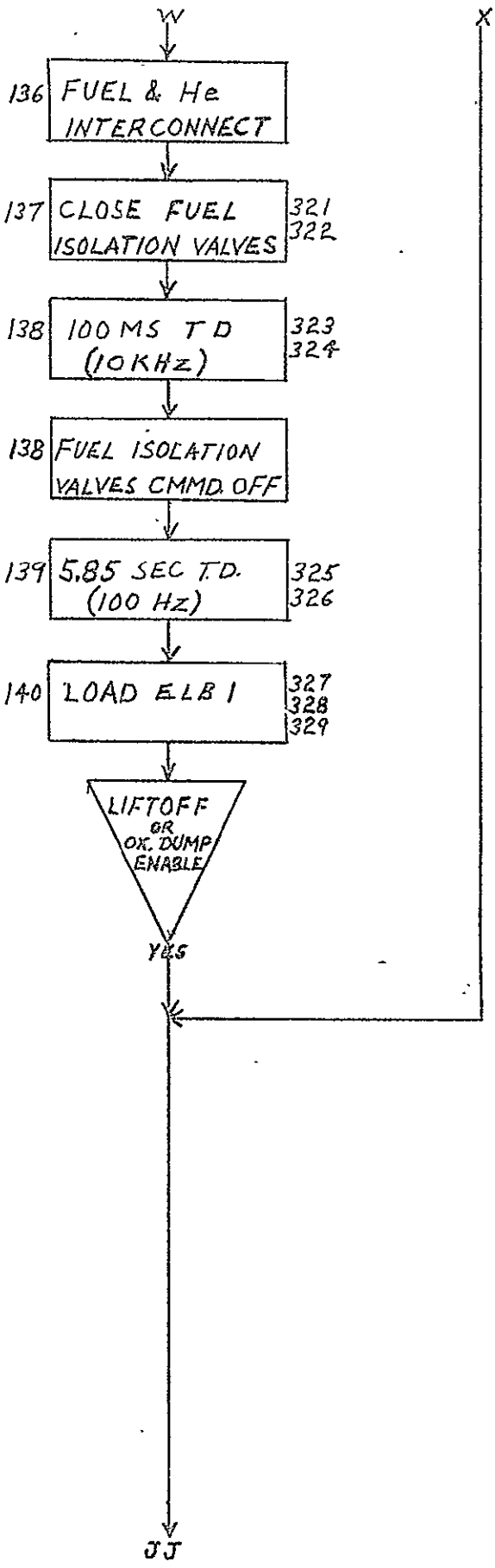


FIGURE 2-2 - Continued

FIGURE 2-2 - Continued

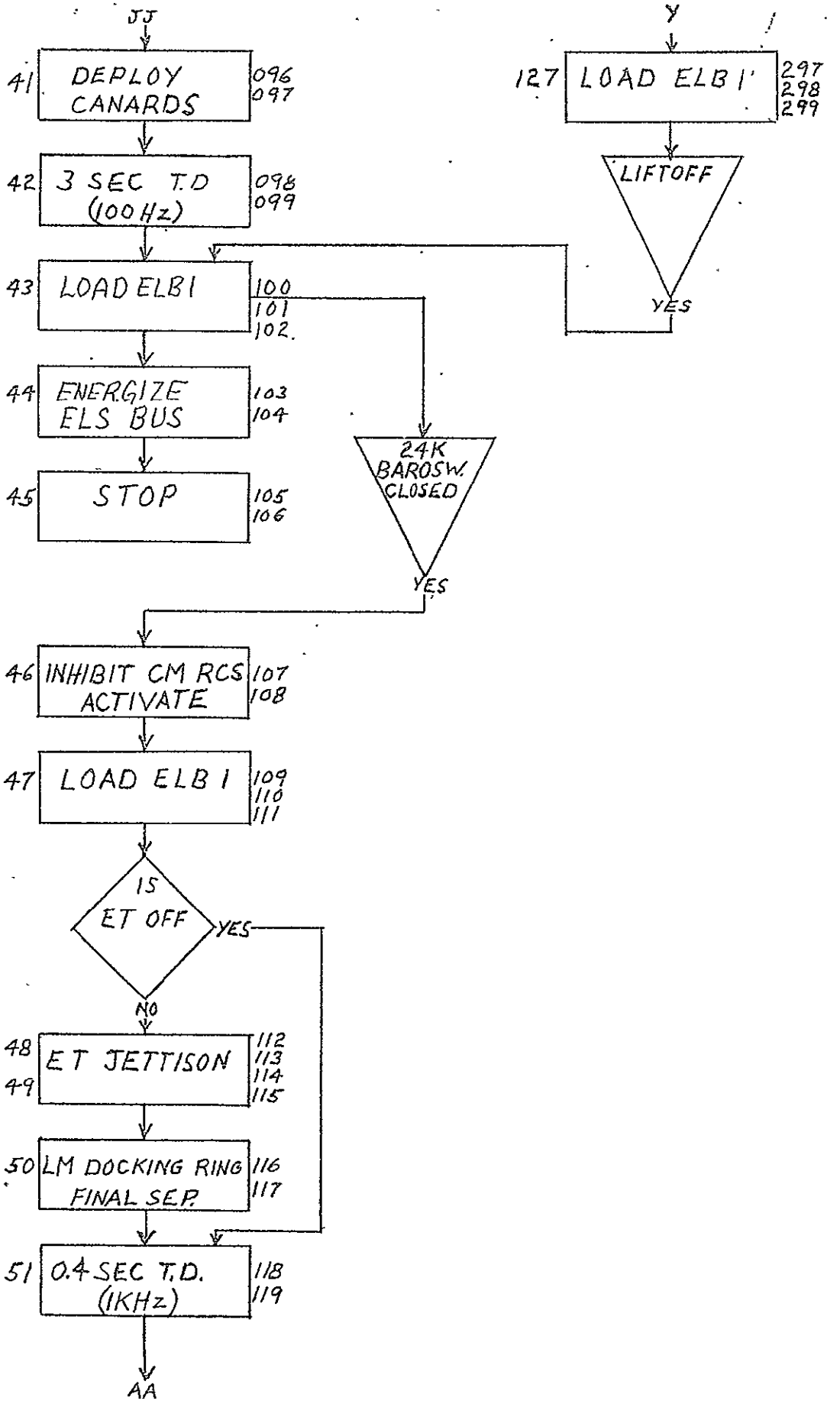


FIGURE 2-2 - Continued

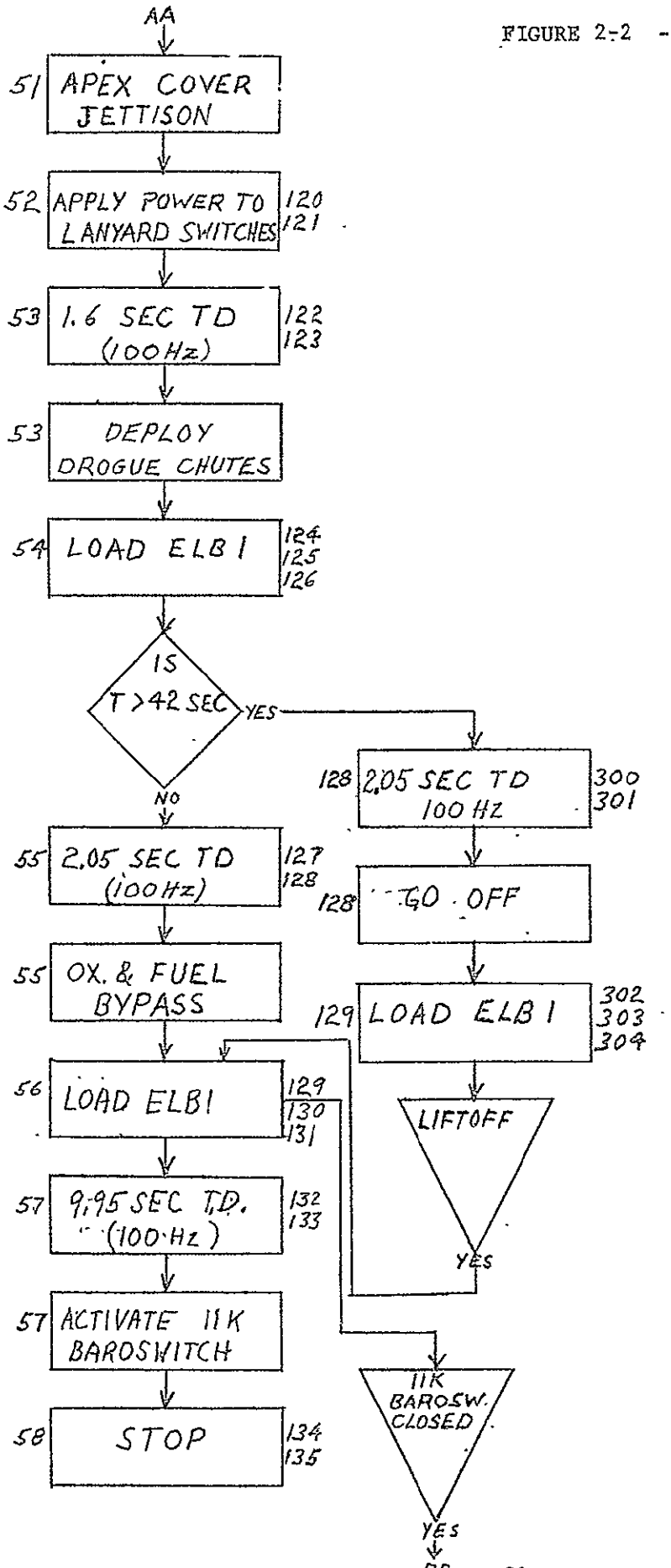
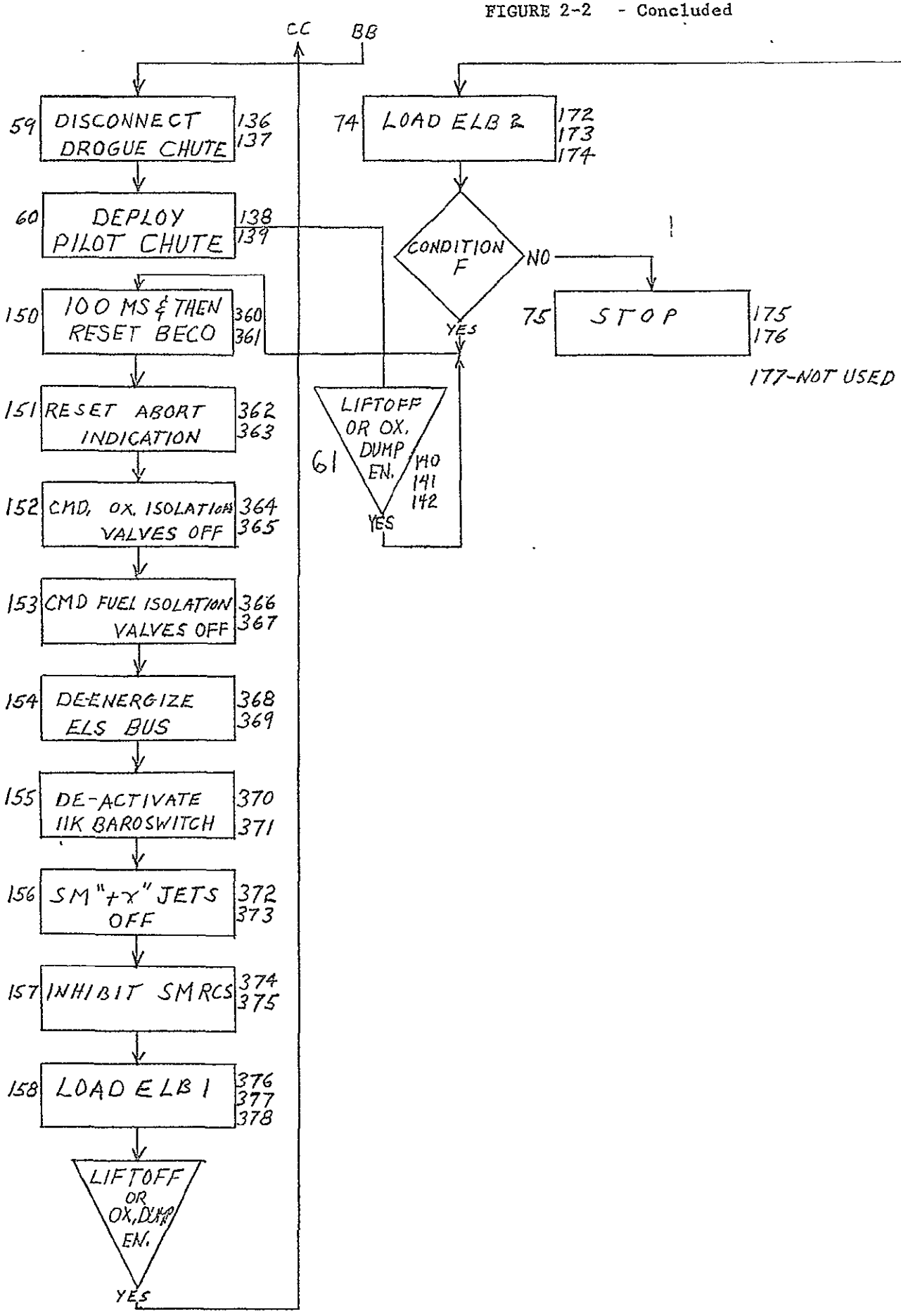


FIGURE 2-2 - Concluded



2.6 Packaging Summary

The size, volume, and weight for the Solid State Sequencer System is shown in the table below.

	Size (in.)	Volume ($in.^3$)	Weight (lb.)
CM Unit	6.6 X 8.2 X 24.6	1330	48
SM Unit	2.3 X 5.4 X 7.50	93	4
System.		2846	104

The CMU is packaged in a machined aluminum housing consisting of a upper housing with a cover and a base housing with a cover shield. These are then fastened together to form the complete unit. To ensure adequate checkout capability and maintainability at the module level, most components are mounted on plug-in type modules.

The upper housing contains the Fuse and Fuse Resistor Modules, the Pyro Timing Circuit Modules, the Output Switching Circuit Modules with low profile components, the Memory Module, the Decoding Logic Module, the CTL Modules and the Integrated Circuit Modules. The modules consist of two printed circuit boards mounted back-to-back on a frame across the top and spacers in between. The connectors are offset on each board and interleaved to conserve headroom. The only exception to this is the PFC Module configuration where the components on each board face one another and are interleaved to conserve headroom. These modules plug into a mother board which provides the power and ground interconnection, the signals are hard wired. The Memory Module is not a plug-in module but is mounted permanently to the housing structure. It consists of eight boards and a memory core in a stock configuration. All P.C. board plug-in modules employ the use of a point-to-point wiring technique covered in document 5000-10. This technique was used to replace printed circuit interconnections reliably, to reduce cost, procurement time and to facilitate making changes during build and final checkout of engineering model.

The base housing contains the power supply and the balance of the output switching circuits. The majority of the output switching components were large and required heat sinking. The base provided the proper environment for these. The power supply is completely shielded from the rest of the unit as is the output switching circuits. The base plugs into the upper housing to interconnect the two parts together.

Pressure relief valves are located at the rear of the case to provide for pressure differential. The external interface connectors are positioned on the front face of the unit. The Fuse and Fuse Resistor Modules are accessible from the outside of the front and top front of the unit.

The SMU is packaged in a low profile machined aluminum case with a top cover. The low power dissipation components are mounted on two printed circuit boards in a stack configuration in the center of the case. The external connectors are at one end and the TO-3 devices are mounted on the other end on two plates in such a manner as to provide a heat path to the base mounting. Other components which require heat sinking are mounted directly to the case below the printed circuit boards. Interconnections are accomplished with a wire harness. The case is designed to provide for the pressure differential.

3. SUBSYSTEM AND CIRCUIT DESIGN

3.1 General

The logic circuitry is a combination of TTL integrated circuits (IC's) and core-transistor logic circuits (CTL's). The latter circuits are used in the time and event logic where constant power must be applied. In addition to low average power dissipation, the CTL circuits provide a memory capability which is needed to re-establish operation after a power dropout. Some low power TTL IC's are also used in areas where constant power must be used and where signal levels must be maintained. The majority of the regular power TTL IC's are only used in those portions of the system which have switched power applied.

3.2 Timer

The timer is designed solely with CTL circuits. It counts down a precision input frequency of 10 KHz to provide additional frequencies of 1 KHz, 100 Hz, and 10 Hz. Any one of these four frequencies may be selected in the program and gated into a twelve stage binary counter to provide the actual time count. The count is controlled by loading the complement of the desired time interval into the counter and counting up to 4096. Then on the next 10 KHz clock pulse an output is generated. Two timers operate in parallel and both must provide an output within 100 microseconds of one another for a sequence to continue. Otherwise a fault indication is generated. A schematic of the timer is shown on schematic 5200-221 in Appendix A, Engineering Drawings.

3.3 Event Logic

Each input event passes through an input filter which provides a nominal 1 millisecond delay to prevent noise from triggering the system. At the end of this time the input filter provides a current pulse output which sets an event CTL in the event logic and provides an event indication input to the sequence generator in Appendix A, Engineering Drawings. The sequence generator generates a set of four interrogate pulses which are used to determine if the event equation has been satisfied and to generate the proper output response from the event logic. If a YES answer is received from the event logic, a branch operation is instituted which results in a branch to a different memory location. The branch address is stored in a separate CTL register schematic 5200-218 in Appendix A, Engineering Drawings.

3.4 Memory System

Contents:

3.4.1 Function

The memory is used to store up to 512 11-bit words. The memory capacity, however, is 1024 12-bit words. The extra bit in the word is a parity bit used for error detection, and the extra 512 work capacity is used to provide functional dual redundancy. This is a random access, 4-wire, coincident current memory using read/restore (R/R) and clear/write (C/W) cycles. Full cycle time is 1.8 microseconds. Access time is 0.4 microseconds.

3.4.2 Program Restrictions

The memory should be operated with a duty cycle limitation such that no more than 1024 memory cycles (R/R and/or C/W) are performed in any 1 second time period. This represents a maximum average duty cycle of about 0.18%. This limitation is imposed by the heat dissipation capabilities of the memory drive circuits, and the current and regulation capabilities of the power supply. Designing drivers for higher duty cycle operation is not required by the system and would adversely affect weight, volume, reliability and cost. Worst case operation from a power dissipation standpoint is to load all zeros continuously in a single memory address location at the maximum permissable duty cycle. While the memory is designed to tolerate this condition, the sequencer system is incapable of generating a condition this severe.

3.4.3 Operation

A simplified schematic of the memory stack is shown in Figures 1A and 1B and a block diagram of the memory system is shown in Figure 2.

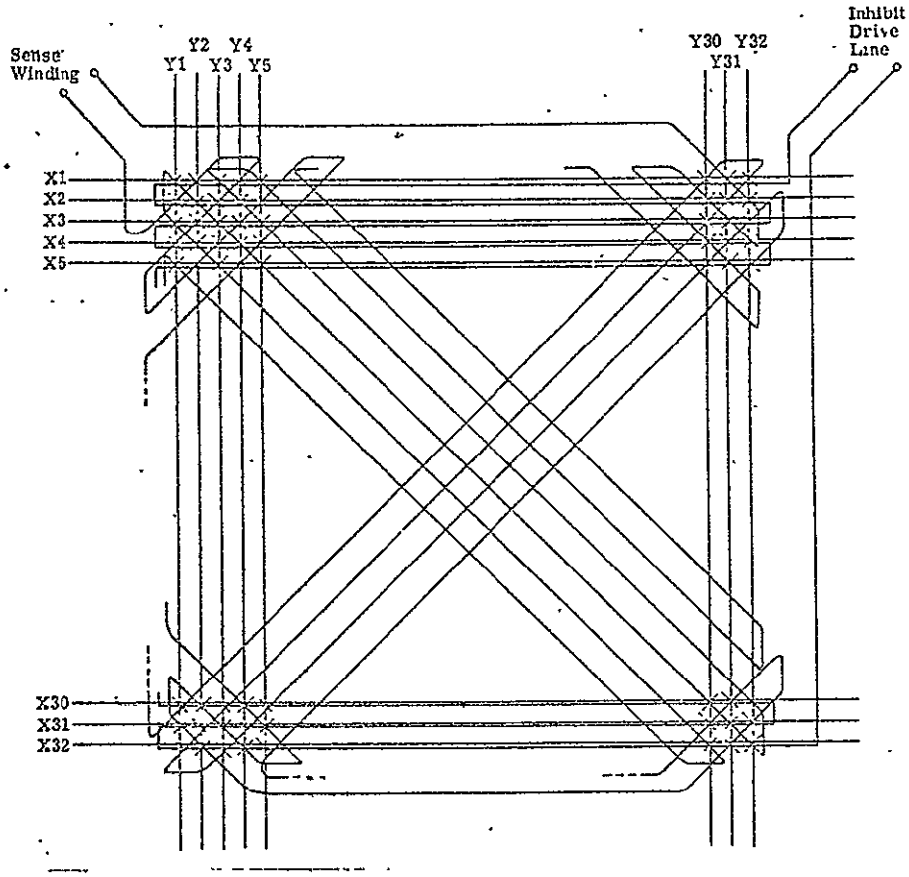


Figure 1A Memory Plane

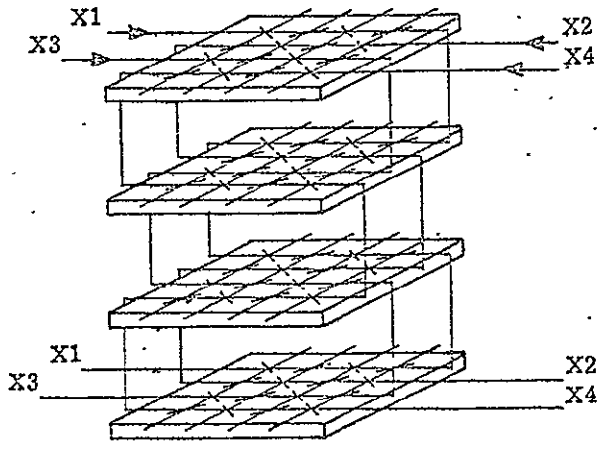


Figure 1B Simplified Stack Interconnection

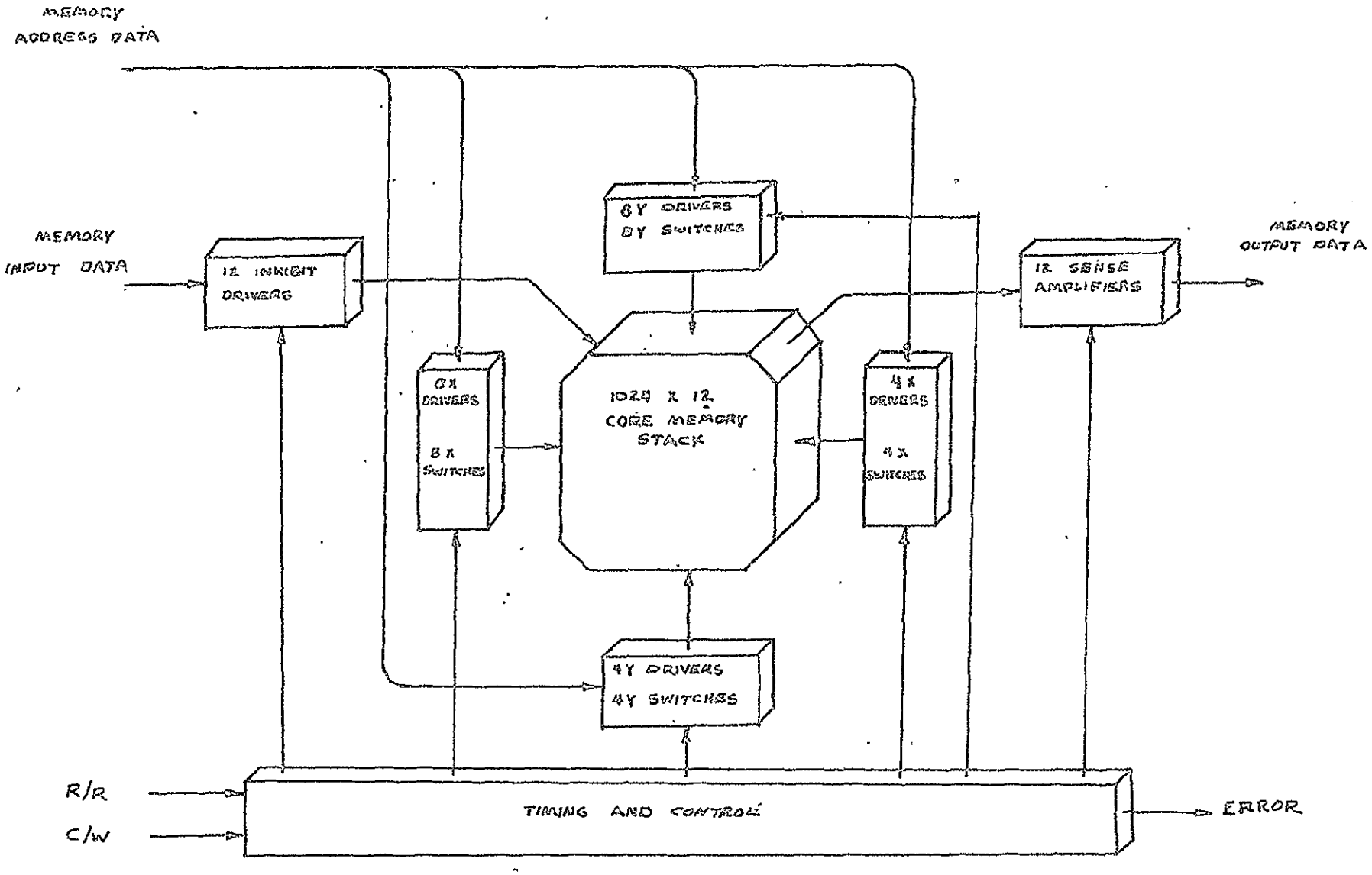


FIG. 2 BLOCK DIAGRAM

A ferrite memory core stores data by retaining flux in either the ONE or ZERO polarity. Data is set into a core by driving a "full drive current" through the core in either the ONE or ZERO direction. (See Figure 3).

The memory system contains 12,288 cores arranged in 12 planes; each plane having 32 rows and 32 columns of cores. The memory has 1024 words (this is the number of cores in each plane) with 12 bits in each word (this is the number of planes). A memory location is determined by selecting one row (x line) and one column (y line). Corresponding x and y lines in all planes are connected in series so this selection selects one core in each of the 12 planes; i.e., one memory word of 12 bits.

Each memory plane has an inhibit winding linking all cores in the plane which is unique to that plane. When this winding is used, a half drive current (one half the current magnitude required to switch a core) is driven in the ZERO direction.

Each memory plane has a sense winding unique to that plane. The two ends of this winding provide the inputs to a sense amplifier. This winding and amplifier is used to detect a voltage generated by the selected core during the unload portion of each memory cycle. If the sense amplifier detects a ONE on the sense line (the voltage generated by a core when it switches) it generates an output signal. The magnitude of a ONE signal on a sense line is from 20 to 70 millivolts. Each plane has 32 x drive lines and 32 y drive lines. Each drive line links the 32 cores in its row or column.

A 12-bit memory word is unloaded from the memory by driving a half drive current through the selected x line and a half drive current through the selected y line. These currents add at the intersections of the selected x and y drive lines in each plane to produce a full drive current through each of the selected cores. The polarity of these currents sets the 12 selected cores to ZEROs. All of the selected cores which had been previously set to a ONE will be switched, and the sense amplifiers for those planes will generate output signals. Selected cores already in state ZERO will produce no voltage in their sense winding since they are not being switched, and their sense amplifiers will, therefore, generate no output signals.

Before loading a 12-bit memory word into a memory location, it is first necessary to unload the data previously written into that location to ensure that all cores are in state ZERO. Half drive currents are then driven through the inhibit windings of each plane into which a zero is to be written, and no inhibit current

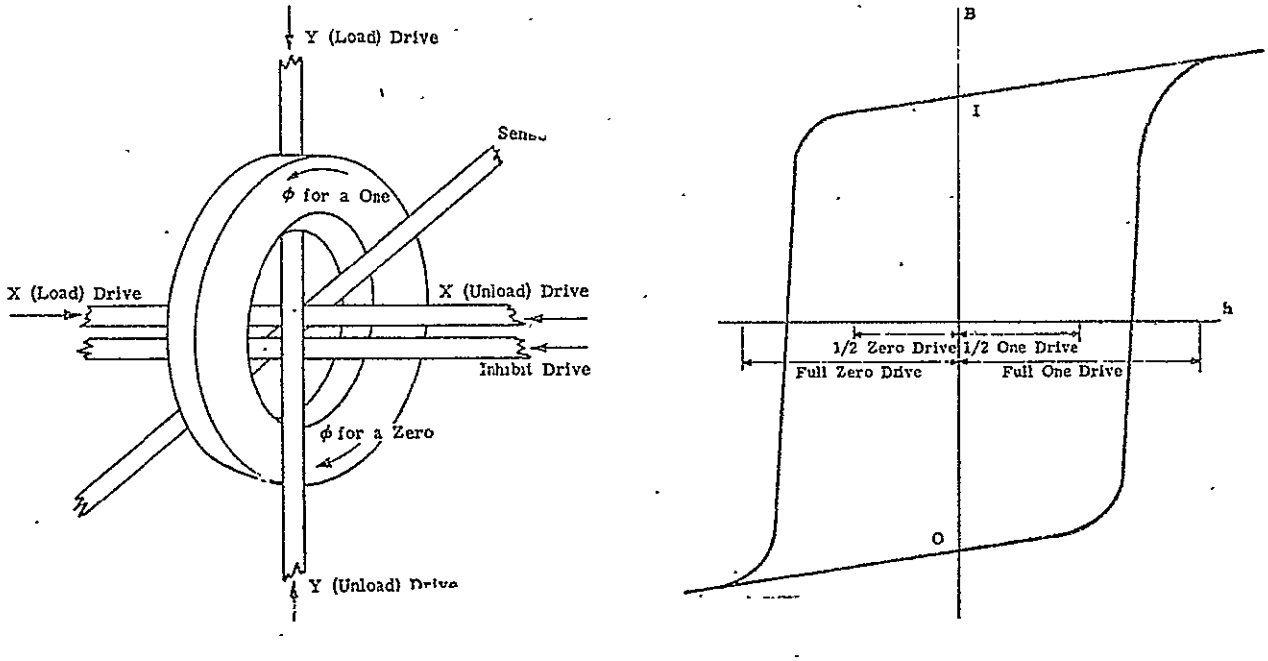


Fig. 3 Memory Core and Ferrite Hysteresis Loop

is driven in those planes where a ONE is to be written. With these inhibit currents still on, half select currents are driven through the selected x and y drive lines as was done for unloading, except that the polarity of these drive currents tend to set the selected cores to ONEs. Selected cores in planes not driven with an inhibit current receive only half a drive current (a half drive tending toward ZERO + a full drive tending toward ONE = a half drive tending toward ONE) and remain in state ZERO. The sense amplifiers are all disabled during the loading operation so that no outputs are generated.

Both the R/R (read/restore) and C/W (clear/write) memory cycles consist of an unload operation followed by a load operation. These two cycles are identical with the single exception that the sense amplifiers are not strobed (remain disabled) during the C/W cycle. A timing diagram of the memory operation is shown in Figure 4.

To drive currents through the selected x drive line during the unload portion of a memory cycle, one x switch is turned on and one x driver is turned on. Turning on the switch connects one side of the selected x drive line to +20 volts. Turning on the driver causes current to be driven from the other end of the selected drive line into ground. A simplified diagram of this drive selection method is shown in Figure 5. To drive currents through the selected drive line during the load portion of the memory cycle, another x switch and x driver are turned on which causes the other end of the selected drive line to be connected to +20 volts, and a regulated waveform of current to be driven from the other end of the same drive line to ground. The driving of the current through the y drive lines is the same as for the x drive lines.

The switches and drivers turned on for a particular memory location are determined by the address transmitted to the memory system on the MEMORY ADDRESS DATA lines (see Figure IV-1), and signals from the timing and control (T&C) section which determine whether the selected memory location is being loaded or unloaded. T&C Logic Diagram is shown on Page 8, Appendix A, Engineering Drawings.

MEMORY INPUT DATA to the 12 inhibit drivers determine which of the inhibit drivers will drive current during the load portion of each memory cycle.

The T&C section generates the necessary timing waveforms to operate the rest of the memory system. R/R and W/W input signals are used to initiate the two memory cycles.

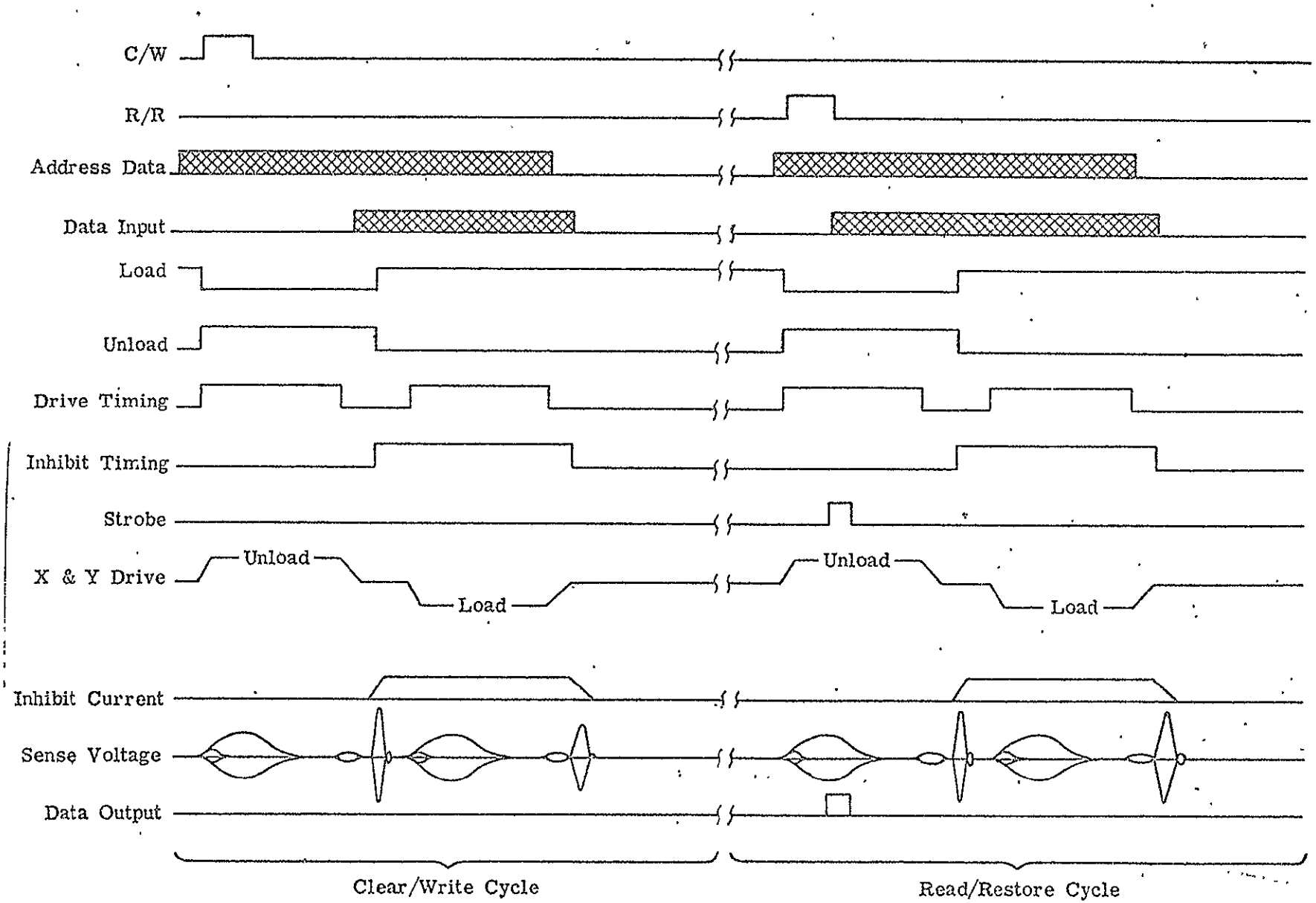


Figure 4 Timing Diagram

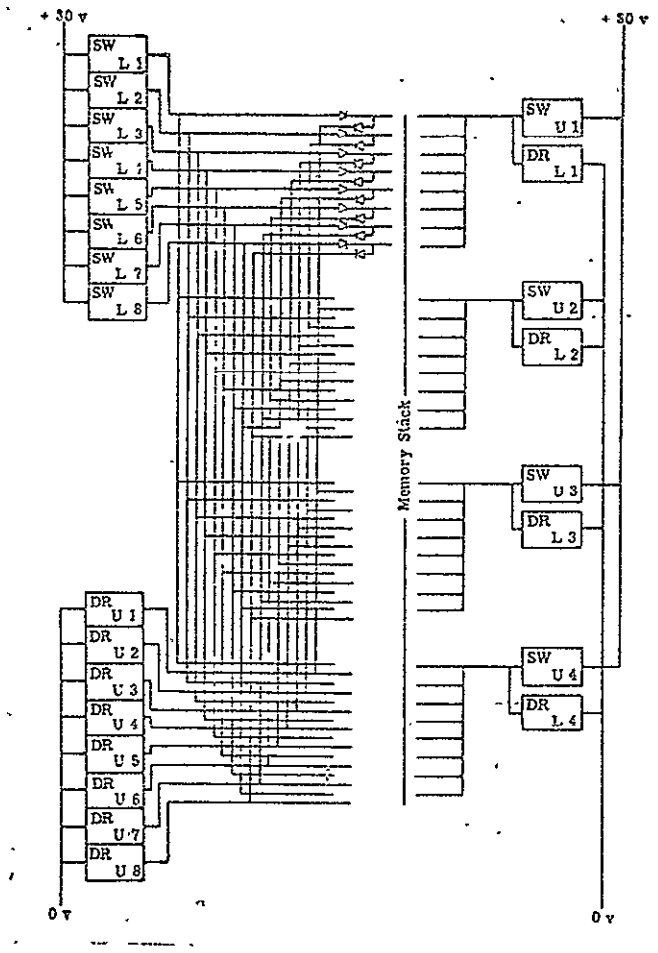


Figure 5 x and y Drive System

3.4.4 Redundancy

Sufficient redundancy is provided within the memory system so that no single component failure can cause the memory system to fail to write and/or read any of the 512 11-bit data words. When a data word is written into the memory, it, plus a parity bit, is written into one of the first 512 memory locations, and the bit complement of that memory word is written into another location in the other half of the memory. This second memory location is obtained by complementing the MEMORY ADDRESS REGISTER, and results in this second memory word using x and y switches and drivers which are entirely different than the x and y switches and drivers used to write or read the first memory word. Because the x and y switches and driver electronics used to write or read one of these two words is not shared with the electronics for the other word, any single failure resulting in the failure of a current to be driven cannot prevent both words from being read from the memory. The design of the drivers themselves is serially redundant so that no single component failure can cause a driver to be inadvertently turned on.

The only redundancy required in the INHIBIT DRIVERS and SENSE AMPLIFIERS is series redundancy in the INHIBIT DRIVERS to prevent excessive current being drawn from the power supply in the event of a failure tending to turn a driver on permanently. Because of parity checking done outside the memory system, a single failure in one of the inhibit or sense circuits, or in one of the inhibit or sense windings, can be detected. When a data word is read from the memory, the first of the two memory words read out is checked for odd parity. If a fault develops on one of the bit channels, it will force that bit channel to always produce a ONE output or a ZERO output. Because the two memory words representing the data word are bit complements of one another, this fault will cause only one of these two memory words to be in error, and that word will be detectable by a simple parity check.

Because the signals from the timing and control section are used in parallel in so many places, no failure in one of these signals can be tolerated. The circuits in TIMING AND CONTROL are, therefore, triple redundant and majority voted. Logic diagrams for the above reference circuits are in Appendix A, Engineering Drawings.

3.4.5 Redundancy Testing

Provisions have been made for adequate testing immediately prior to launch to verify that no single component failure can cause

an inadvertent output from either of the solid state sequence systems (SSSS) channels.

Within the memory system this provision has taken the form of a set of logic circuits which monitor the T&C timing elements to verify that no element has drifted out of tolerance. The need for this monitoring is explained as follows:

> Assume one timing element -- such as one of the three redundant one shots controlling strobe timing to the sense amplifiers -- had drifted out of tolerance. The situation would then exist where the single failure of one more of these three redundant timing elements drifting out of tolerance in the same direction would cause the majority voted strobe timing signal to the sense amplifiers to drift out of tolerance. This type of failure could cause any number of errors to occur in memory words being read from the memory. Clearly, this condition could result in inadvertent outputs from one of the SSSS channels.

While a component drifting out of tolerance has not generally been considered as a failure mode in other parts of the system or memory, it has been so considered here because of the critical importance of these timing elements.

As part of the prelaunch test to verify redundancy, we plan to exercise the memory by cycling through all memory addresses, and checking parity for all memory words. This test will check all sense amplifier circuits; it will check all of the core memory stack; it will check all of the inhibit drivers, x switches, y switches, x drivers and y drivers for open circuits. This test will not check these drivers and switches for shorted transistors. This test is adequate, however, since an analysis shows that a short in one of these drivers or switches cannot cause an inadvertent output from one of the SSSS channels.

3.4.6 Detailed Circuit Descriptions

The operating temperature range of the Solid State Sequencer System is 0 to 160°F (-17.8 to 71.1°C). This is the temperature of the frame to which this system is mounted.

We have assumed that for any transistor in the memory which dissipates less than 4 mw, the maximum ΔT from transistor case to the system case will be 8.9°C. This gives an operating transistor case temperature range of -17.8°C to +80°C.

Power supply voltages are assumed to have $\pm 3\%$ tolerance or better for constant loads. When high currents are drawn from the memory, capacitors on the power supply lines will furnish the required current and these voltages will then droop beyond the 3% tolerance limits. 10% droop will be permitted on the +26 and +20 volt lines.

3.4.6.1 Memory Stack

The memory stack is an assembly purchased to specification, on pages 40 & 41. Acceptance tests for this stack will be performed at the manufacturers plant.

3.4.6.2 Timing and Control

The timing and control section consists of the timing section, and the majority vote circuits and timing redundancy check circuits shown on schematic 5400-48, Appendix A, Engineering Drawings.

Each set of eight one-shots is used to generate the waveforms L (Load), U (Unload), LDT (Load Drive Timing), UDT (Unload Drive Timing), and S (Strobe). A timing diagram showing these five waveforms is shown in Figure 4.

A majority vote circuit performs its majority vote function on three corresponding one-shots (i.e., S-A, S-B, and S-C) and transmits its output(s) to other memory circuits. Each majority vote circuit is dual redundant and the two outputs (i.e., S_1 and S_2) are compared using an exclusive OR circuit. The outputs of the four exclusive OR gates are OR'd together to generate the T&C FAULT output.

The majority vote circuits, therefore, correct for any single component failure in the T&C circuits, but perform no error correction for faults in the majority vote circuits themselves. The dual redundancy provides for the detection of any single component failure.

3.4.6.3 Switches (Appendix A, Engineering Drawings, Schematics 5400-42, 43, 44, 45, 46)

A schematic of the output section of a switch circuit is shown in Fig. 6. Inputs to the switch are from TTL integrated circuits. When inputs are low, all transistors are off. When inputs are high, all transistors are on, and current may be drawn from the +22V supply through Q2 and Q4 into the output. The circuit (Fig. 6) shows how a memory drive line is connected to +22 volts through this switch circuit, and a current driven to ground from the other side of the line.

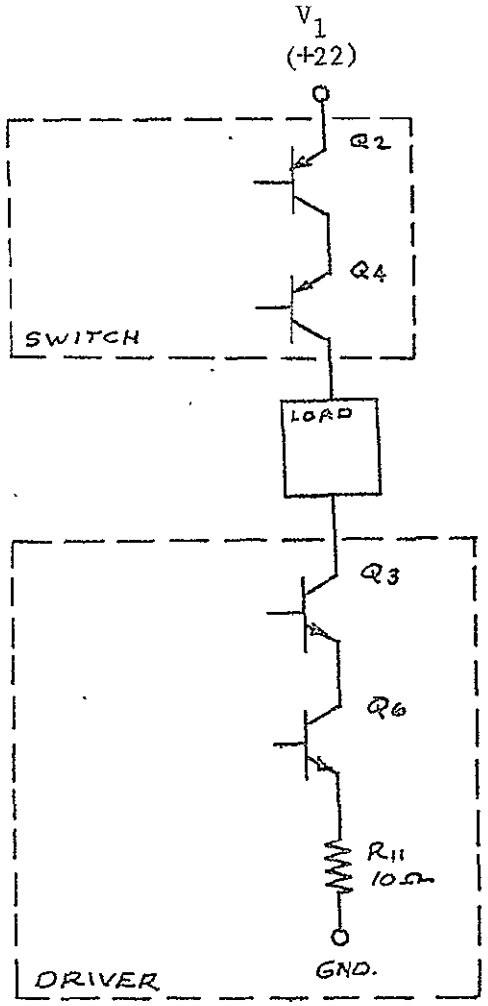


FIG. 6

SPECIFICATION FOR FERRITE CORE MEMORY STACK

1.0 Capacity - The memory stack shall have a storage capacity of 12,288 bits consisting of 1024 words of 12 bits each.

2.0 Wiring Configuration - Wiring of the stack shall be a standard 4-wire configuration for coincident current operation consisting of X, Y, inhibit and diagonal sense.

3.0 Decoding Diodes - The stack shall include the address decoding diodes; two diodes per line. The X and Y drive lines shall be wired as shown in Figure 5. The diodes used shall have been proven in previous space or aircraft programs. "Hi-rel" diodes are not required, but the diodes used shall be available in a "hi-rel" version. "Hi-rel" parts will be required for any follow-on effort involving a production run of flight hardware.

4.0 Cores - The ferrite cores used shall be Electronic Memories' Lithium 34-104-1 or equivalent.

5.0 Volume - The volume of the stack shall not exceed 25 cubic inches

6.0 Weight - The weight of the stack shall not exceed 18 ounces.

7.0 Environmental

7.1 Operating Life - Sixty days nominal flight time + test time including factory checkout, acceptance tests, pre-launch, etc.

7.2 Temperature Limits - Operating ambient 0 to 160 F $\pm$ 5 F.

7.3 Thermal Vacuum - The stack will be exposed to a vacuum of 1.0×10^{-5} mm. Hg. The stack shall perform all required functions over the temperature range given in 7.2.

7.4 Shock - The stack shall be capable of withstanding a shock of maximum amplitude of 30 g $\pm$ 10% while operating. The shock waveform shall be a sawtooth with an 11 millisecond rise time and a 1 millisecond decay. The stack shall continue to operate within tolerance during and after the shock. The shock shall be in two directions for each of three mutually perpendicular axes.

7.4.1 - Non-Operating - The shock waveform shall be as in 7.4 except that the peak shall be 78 g $\pm$ 10%. The unit is not required to operate during or after this test, but it shall maintain structural integrity. Shock shall be in two directions for each of three mutually perpendicular axes.

7.5 Vibration - Random vibration - Operating linear increase in 3 DB/octave steps from 0.015 g^2/cps at 20 cps to 0.06 g^2/cps from 80 cps. Constant at 0.06 g^2/cps from 80 cps to 2000 cps. (Vibration in each of 3 mutually perpendicular axes for 5 + 1 -0 minutes in each axis.)

7.6 Acoustic Susceptibility - The stack shall be capable of withstanding a sound pressure level of 140 db overall with a frequency range of 4.7 to 9600 cps.

7.7 Acceleration - The stack shall be capable of withstanding 20 g's $\pm$ 1 g in two directions for each of three mutually perpendicular axes, 5 ($\pm$0) minutes in each direction. The unit shall be capable of operating during the after exposure to these conditions.

7.8 Shelf Life - The shelf life of the stack shall be a minimum of 5 years.

3.4.6.4 Drivers (Appendix A, Engineering Drawings, Schematic 5400-43, 43, 44, 45, 46)

A schematic of a driver circuit is shown on 5400-42. Inputs are from TTL micrologic. When both inputs are low, all transistors are off. When the inputs are high, all transistors are on, and a controlled current is driven from the output line into 0 volts.

When the inputs go high, the input transistors Q1 and Q4 switch on, which in turn turns on Q2 and Q5. These four transistors switch on rapidly. C2 and C4 begin charging through R2 and R9 toward +26V. When this charge reaches a certain magnitude, it is clamped by CR3 and CR4 to the clamp voltage.

When the inputs go low, Q1, Q2, Q4 and Q5 switch off rapidly. The charge on C2 and C4 begins discharging toward -12 volts. When this charge reaches a point slightly below ground, it is clamped by CR2 and CR5 to about 0 volts.

The output transistors Q3 and Q6 act as emitter followers causing a current waveform of the same shape as the voltage waveforms on C2 and C4 to be driven through R7. C2 and C4 together with R2 and R9 control the rise time of the output drive current; which is about 100 ns. C2 and C4 together with R3 and R5 control the fall time of the output drive current, which is about 100 ns. The duration of the output is controlled by the duration of the input voltages. The magnitude of the output drive current is controlled by the magnitude of the clamp voltage.

The ferrite cores being driven by these currents require the drive currents to vary with temperature. The magnitude of these currents is fixed by the clamp voltage, V_c and is given by:

$$I = (V_c - .615)/11.53$$

The range of clamp voltages over which the memory will function correctly was determined experimentally and is shown in Figure 7.

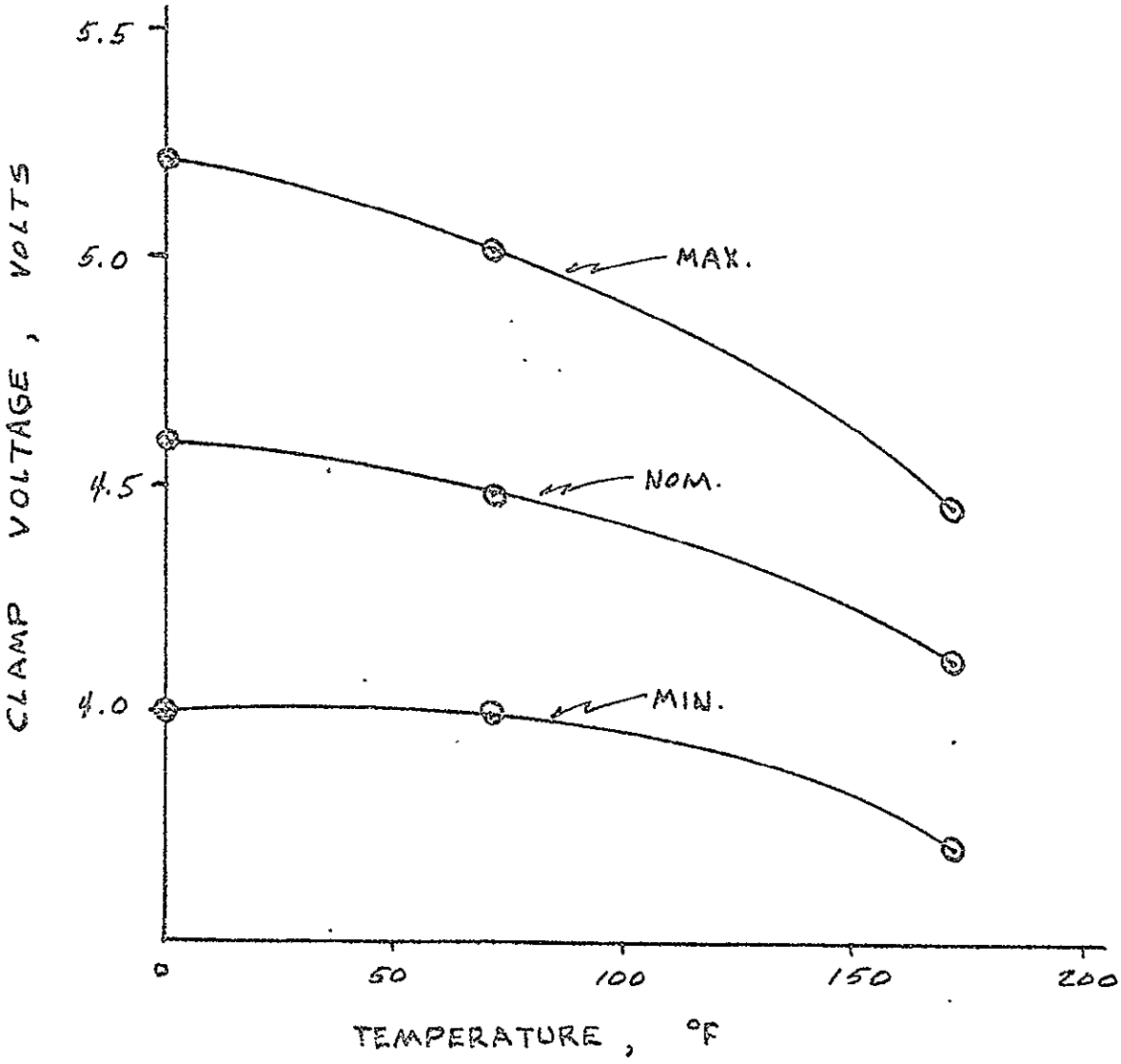


FIG. 7

3.4.6.5 Sense Amplifiers (Appendix A, Engineering Drawings, Schematic 5400-44)

The sense amplifiers consist of Fairchild's μA711 dual comparators together with a resistor network. This network sets a threshold voltage on the inputs of the two comparators. The two comparators are connected to detect sense voltages of either polarity whose magnitude exceeds the threshold voltage.

3.5 Decoding Logic

A block diagram of the decoding logic is shown in Figure 8. This circuitry is duplicated within each channel to protect against inadvertent outputs due to a single component failure. Both sets of decoding logic must provide an output to turn on an output switch.

When a program word is read from the memory, the command portion (6 bits) of that word is set into the command register. Upon completion of the associated time count, a signal is sent from the timer to the input of the decoder driver. The decoder driver generates current pulses which initiate the decoding operation, resulting in a current pulse being steered down 1 of 64 possible paths under direction of the decoding matrix. This is the pulse which provides the set (or reset) input to the latching circuits. After this operation, a reset pulse is generated for the purpose of resetting the input cores on the 0.125 sec. latching circuits and the pyro-firing circuits.

Since the current pulses supplied by the decoding logic are of short duration (4 microseconds), power interruptions (greater than 500 microseconds) will reset any output switches which are in the "ON" state to the OFF state. To force the output switches back to their operating condition prior to the power interruption, a reset pulse is generated by the Power Up Reset Circuit. The functioning of this pulse is described in the output switch section.

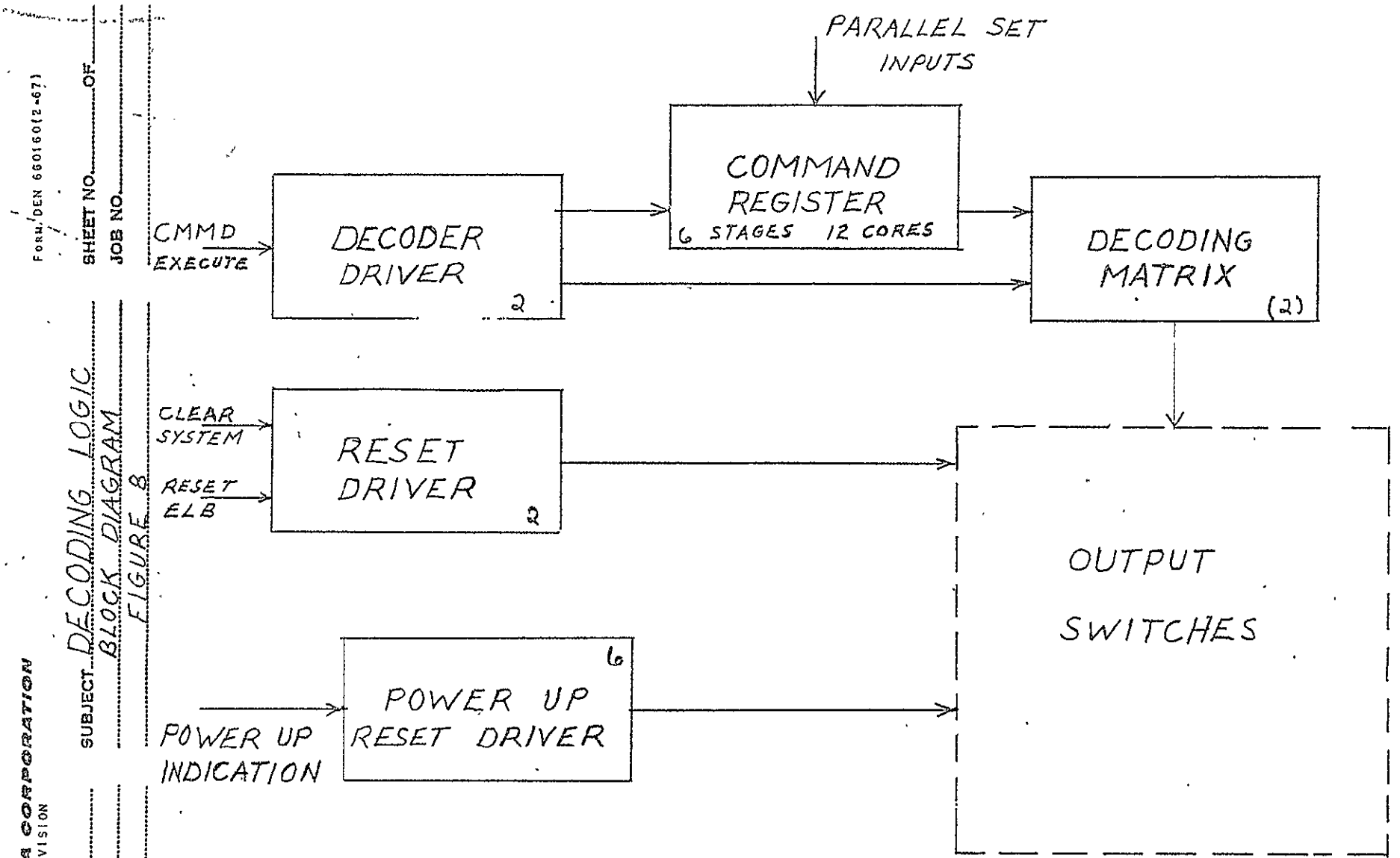
Since the decoding logic uses pulse type logic, operating at a very low duty cycle, power considerations are non-existent, all resistors are 1%, 1/8 watt metal film. All cores are tape wound permalloy square loop on stainless steel bobbins, Magnetics, Inc. P/N 80529-½DMA, and are oil filled to provide viscous damping as protection against the vibration and shock environment. All capacitors are ± 10% ceramic.

All circuits shown here have been breadboarded and tested from -30°C to +100°C with satisfactory operation.

Schematics of the decoding logic are given in 5200-213, 214 of Appendix A, Engineering Drawings. For the following discussion 5200-214 will be used as a reference.

Decoder Driver

An input signal turns on Q1, causing current to flow through a 4 turn winding on T1. This current causes T1 to switch, generating a positive voltage on a 30 turn winding which keeps Q1 on after the input pulse has disappeared. When Q1 is on, a positive voltage appears across R5 which turns on Q2, thereby discharging C3. When T1 has completely switched, Q1 turns off, Q2 turns off, and C3 charges up causing Q3 to turn on. The same process is repeated except that the current pulse drawn through Q3 causes T1 to switch back to its original condition. The circuit is then ready to receive another input pulse. Since the width of the current pulses generated by this circuit are dependent on the switching characteristics of T1, and since the cores driven by these pulses have the same



MARTIN MARIETTA CORPORATION
DENVER DIVISION

FORM DEN 66016012-67)

BY.....DATE.....
CHKD. BY.....DATE.....

SUBJECT DECODING LOGIC BLOCK DIAGRAM FIGURE 8

SHEET NO.....OF.....
JOB NO.....

part number, variations in switching characteristics due to temperature changes are automatically compensated for. The current pulse amplitude is set by CR2, R5 and CR6, R11. R5 and R10 are initially selected to provide compensation for the individual voltage variations in CR2, Q1 and CR6, Q3.

Command Register

Commands are entered in parallel from the set circuitry shown on schematic 5200-230 which provides a ground at either the SET 1 or the SET 0 terminal for each stage. This current sets one core and assures that the other core is reset. When the Decoder Driver is turned on, the information in each half of the register (3 stages) is used to set one core in an eight core decoding submatrix.

Decoding Submatrix

The decoding operation is performed by two decoding submatrices of eight cores each. The information in 3 stages of the Command Register is used to steer a current pulse through 1 of 64 possible paths. This current pulse flowing through a core winding inserted in the path generates a voltage which turns on one of the output latching circuits.

Reset Driver

This circuit receives inputs from the external system clear switch and from the Reset ELB drivers. The Reset Driver generates a pulse approximately 20 microseconds wide and 150 milliamperes in amplitude. This pulse is used to reset the input cores for the Pyro Firing Circuits and the 0.125 Sec. Latching Circuits.

Power Up Reset Circuit

Whenever power is applied to the system, this circuit receives an input which causes it to generate an output pulse, 4 microseconds in duration and 235 milliamperes in amplitude. This pulse is applied to the memory cores in the latching circuits causing any latching circuits which had been ON prior to the power interruption to be returned to the ON condition.

3.6 Output Switches

All output switches except for the Pyro Arming Circuit are series redundant to protect against an inadvertent output due to any one component failure. The inputs to the switches come from two separate decoding matrices, A and A'. With the exception of the Pyro Firing Circuits, these input signals are used to activate transistor latching circuits which in turn drive the power output stages. Two types of latching circuits are used: one is a 125 millisecond latch which automatically resets after that period of time; the second type stays latched until turned off by a separate input signal. The former

type is used to drive the Pyro Arming Circuits and the Motor Switch Driver Circuits; the latter is used for all other output drivers.

The different types of output drivers are:

Circuit	No./Channel CM Unit	No./Channel SMJC
1. Pyro Arming Circuit	2	-
2. Pyro Firing Circuit	28	-
3. Motor Switch Driver	2	-
4. Solenoid Driver	4	4
5. 100 Milliampere Switch	4	-
6. 0.5 Amp Switch	2	-
7. BECO Circuit	1	-

In most instances the power transistors used in the above circuits have a BV_{CBO} = 100V and a BV_{CEO} = 80V. To protect against transients, (80V on top of a 30VDC level) and to provide a 50% safety factor, transistors with a BV_{CEO} = 165V would be required. To circumvent this, 50V zener diodes will be placed across the logic and pyro busses. These are 10W devices manufactured by Unitrode (P/N UZ7850), which have a surge rating of 20 amperes for 500 microseconds. Four of these devices are used in parallel across each bus. This is sufficient to keep the bus voltage from rising above 56V, thereby permitting the use of transistors with BV_{CEO} = 80V.

All of the output switches have been designed for operation at 1.5 times the specified maximum line voltage. Under this condition, the currents are also about 1.5 times the operating maximum and the voltage is 2.25 times the maximum seen in actual operation.

Output Latch Circuit (Appendix A, Engineering Drawings, 5200-205

This circuit turns on when a current pulse from a decoding matrix is applied to the SET input. This pulse causes core, T1, to switch thereby generating a positive voltage on the twelve turn winding which is connected through CR11 and R13 to the base of Q3. This voltage pulse causes Q3 to turn on, which in turn causes Q1 to turn on, producing a positive voltage at the collector of Q1 which feeds back through R10 to cause the circuit to latch up. At the same time a minimum of 5 milliamperes of current is fed through R6, R5 and a 20 turn winding on T2. This causes T2 to switch to the set state, thereby providing a "memory" that this particular latching circuit has received a set command. If power is interrupted, at the conclusion of the interruption the latching circuit will be in the OFF condition. The return of power is sensed by the Power Dropout Timer Circuit which provides an input signal to the Power Up Reset Circuit which, in turn, generates a Power Up Reset Pulse. This pulse travels through the memory cores in all

of the latching circuits, causing the memory cores, in the circuits which had been on, to switch, thereby returning the circuits to their condition at the time of the power interruption. Since the signal from the Power Dropout Timer Circuit may not be generated for short term transients, an isolation diode, CR2, and a hold up capacitor, C1, are used to protect against this condition.

To turn the latching circuit off, a current pulse is applied to the RESET input. This pulse resets both cores T1 and T2. When core, T1, resets, a positive signal is applied through CR13 and R15 to the base of Q5, causing Q5 to saturate. This drops the voltage on the base of Q3 to the point where Q3 turns off thereby unlatching the circuit.

This circuit will supply up to 25 ma. of output current at a logic bus voltage of 20V. Thus, it can drive several output switches if required.

0.125 Sec. Latch Circuit (Appendix A, Engineering Drawings, 5200-208

This circuit is similar to the Output Latch Circuit except that it contains a unijunction timing circuit which automatically turns it off in a nominal 0.125 sec. Under worst conditions it will remain on for at least 0.10 sec.

Pyro Arming Circuit (PAC) (Appendix A, Engineering Drawings, 5300-41

This circuit is used to supply power for a number of pyro firing circuits, only one of which may be turned on at one time. The PAC is turned on by 0.125 Sec. Latching Circuits. Separate outputs are provided to supply power to the master and slave SCR's in the Pyro Firing Circuit. CR1 and C1 provide protection against negative transients on the Pyro Bus which would tend to turn off the Pyro Firing Circuit. Each PAC can supply enough power to fire two pyros simultaneously.

Pyro Firing Circuit (PFC) (Appendix A, Engineering Drawings, 5200-203

The pulse supplied by the decoding matrix is about 4 microseconds in duration. This is not long enough to guarantee turn on of the 2N684's. Therefore, a master-slave arrangement has been used. The master SCR's (2N2325A) turn on within 1 microsecond. An inductance, L1, is used in the output circuit to protect the slave SCR's from harmful di/dt effects. This output circuit is identical to the one designed and proven for Titan III. Each PFC can fire two pyros simultaneously.

Motor Switch Driver (MSD) (Appendix A, Engineering Drawings, 5300-41

This circuit is basically a redundant version of the PAC except that transistors with a higher BV_{CEO} rating are used. The MSD will drive two motor switches in parallel. It is turned on by 0.12 sec. latching circuits.

Solenoid Driver (SD) (Appendix A, Engineering Drawings, 5300-41)

The SD has been designed to drive two CM solenoids in parallel. Since these solenoids have a lower impedance than the SM solenoids, this circuit is suitable for both applications. The inputs to the solenoid driver are supplied from latching circuits which must be turned off by command. To protect the output transistors from the inductive kickback voltage when the circuit is turned off and still provide a fast dropout capability in the SM application, a 27 volt zener diode with a high surge rating is used. To reduce the required voltage rating on the output transistors, three 50V zener diodes are used across the bus in the SM unit for transient suppression. With the 50% safety factor added in, transistors with a BV_{CEO} of about 130V are required. The 2N4071 and MM4545 transistors used in this application more than meet this requirement. In the CM unit the zener diode is not required and a 1N4942 diode is used to suppress negative transients. Therefore, the output transistors may have lower breakdown voltage ratings and 2N4070 and 2N4031 transistors are used in this application.

100 Milliampere Switch (Appendix A, Engineering Drawings, 5200-206)

This circuit is used for several different low power applications none of which require as much as 100 milliamperes. However, since the switch could be designed for this capacity using the same type components, this was done to provide added flexibility. Inputs to this circuit are supplied from latching circuits which must be turned off by command.

0.5 Amp Switch (Appendix A, Engineering Drawings, 5300-41)

This switch is designed to supply 0.5 amp to the SCS. In design, it is similar to the 100 milliampere switch except that transistors with a higher current rating are used in the output stage. Inputs to this circuit are from a latching circuit which is turned on and off by commands.

3.7 CTL Description

Figure 9 shows the circuit schematic of the CTL element. The terminals a, b, and c shown with dotted lines between them are connected to core windings when used to perform logic operations. The windings may be on the core of this element or the core of some other CTL element, depending on the required logic operation to be performed. For the purposes of an approximate initial description of the CTL circuit operation, the impedances of the core windings between these terminals is considered negligible.

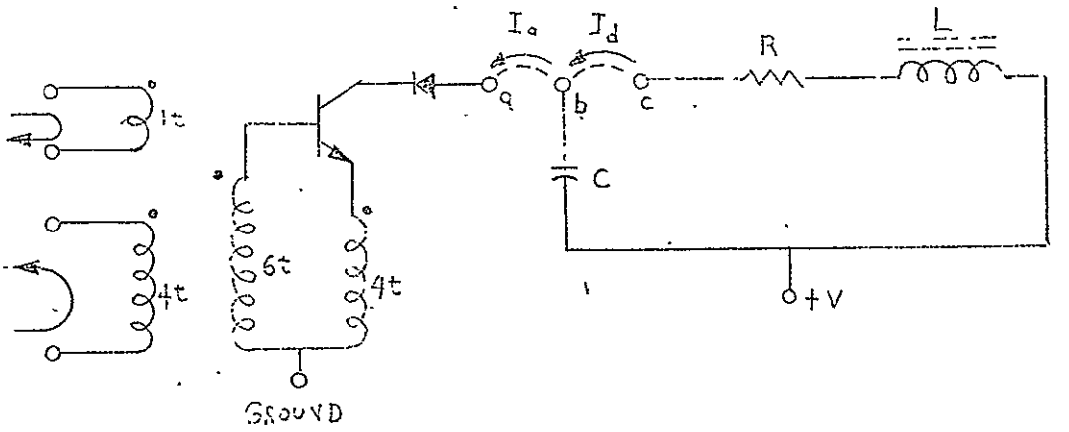


Figure 9 CTL Circuit Schematic

The core is always left in one of two magnetic states -- a ZERO or a ONE. It is forced into the ONE state by driving a current through the 4-turn input winding. The polarity of this current is as shown in Figure 5.1 and the amplitude of the current is about 150 milliamperes. When the core changes state (switches) from a ZERO state to a ONE state, voltages are generated on all the windings of the core. The polarity of these voltages is such that the transistor is not turned on (turned further off).

The core is placed in the ZERO state by driving a current through the 1-turn input winding with the polarity shown. If the core was previously in a ONE state, the core will begin to switch and generate voltages on its windings with polarities that turn the associated transistor on. The resulting emitter current aids in clearing the core (switching the core to a ZERO state) and is regenerative because of the transistor gain. The amplitude of the collector current pulse is about 1.5 amperes, and the base current pulse is about 0.5 ampere.

The output advance current, I_a, lasts for about 0.25 microsecond and charges capacitor C. The RL time constant is such that little of the current I_a comes from the supply plus voltage. Because of the large magnitude of the transistor base current, the transistor charge storage time holds the transistor on even after the core has fully switched, so the capacitor becomes fully charged. The transistor discharges through the resistor/inductor combination producing the delayed output current I_d.

The timing waveform for a CTL is shown in Figure 10. If the core is in the ZERO state at the time the input advance current is driven, no voltage signals will be generated on the core's windings and the transistor will not be turned on.

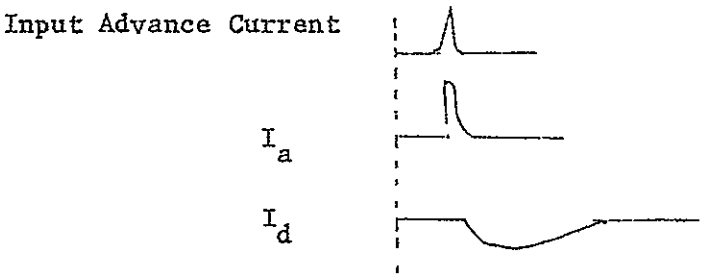


Figure 10 CTL Timing Waveform

Figure 11 shows the logic symbol used to represent the CTL circuit. The advance and set inputs and advance and delayed outputs are those described previously. The inhibit input is identical to the set input, but is of opposite polarity.

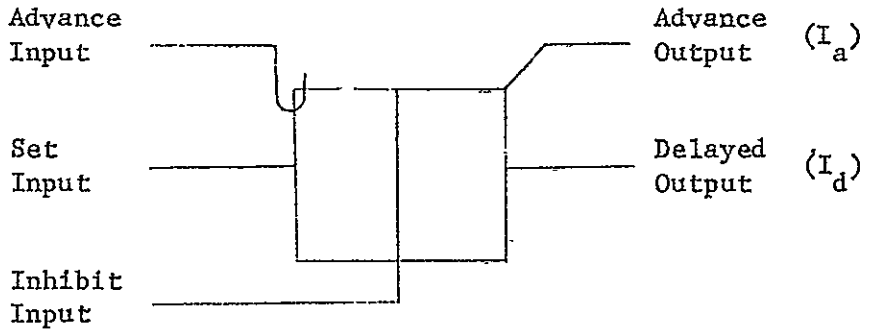


Figure 11 CTL Logic Symbol

A shift register utilizing CTLs is shown in Figure 12. Here the shift windings of all CTLs are tied in series so the shift signal affects all CTLs equally. (The parallel connection shown on the logic diagram indicates that the shift signal is applied equally to each CTL and does not indicate parallel wiring connections.) In operation, I_d from stage 1 provides the set input for stage 2 and I_d from stage 2 provides the set input for stage 3, etc.

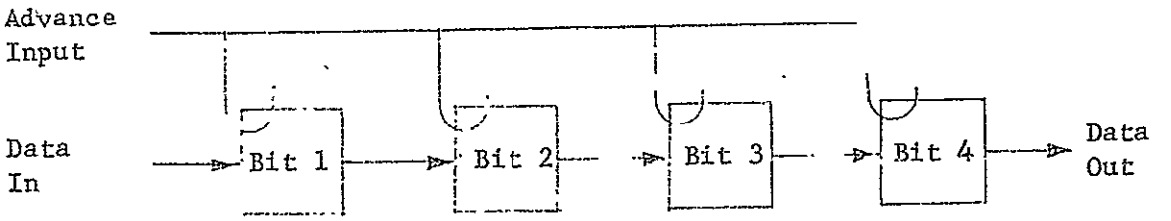


Figure 12 4-Bit Shift Register

A ONE generator using CTLs is shown in Figure 13

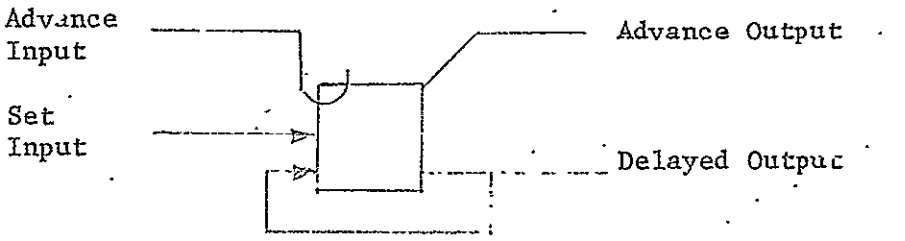


Figure 13 ONE Generator

This element has two set input windings. One of them is connected in series with the delayed output so I_d is driven through it. Once a ONE is set into the core, the circuit will produce a ONE for each advance input since the circuit provides its own set input.

A 4-bit counter is shown in Figure 14

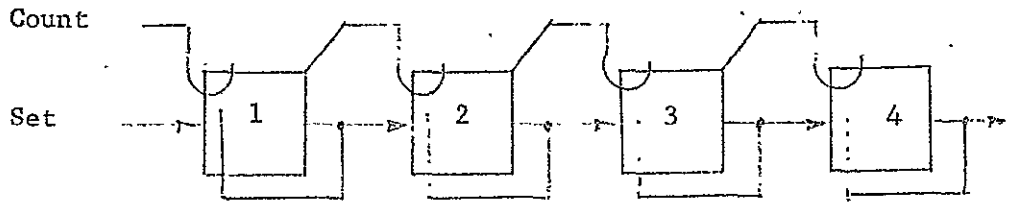


Figure 14 4-Bit Counter

To operate the counter, signals are driven alternately on the count and set inputs, i.e., I_d from CTL-1 is driven in series through the inhibit winding of CTL-1 and the set winding of CTL-2; I_d from CTL-2 is driven in series through the inhibit winding of CTL-2 and the set input of CTL-3; etc. Note that an inhibit current should never be driven when the CTL core is in state ONE. This would have the same effect as driving the advance input.

A majority vote circuit is shown in Figure 15. This circuit has multiple set and inhibit input windings. Circuit operation is as follows. All input signals are driven simultaneously on the five input lines. An interrogate input is then driven. If there are more set signals, an output will be produced. If there are more inhibit signals than set signals, no output will be produced.

These circuits are examples of some of the many logic functions that can be mechanized with CTL elements.

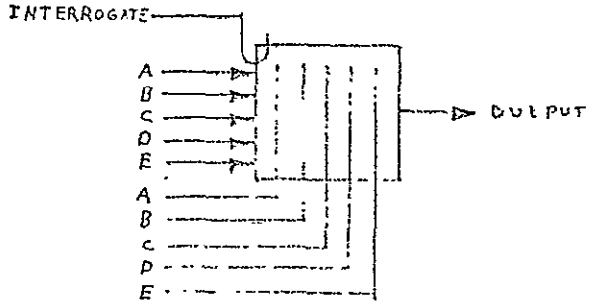


Figure 15 Majority Vote Circuit

4. ENVIRONMENTAL ANALYSIS

4.1 Thermal Vacumn

In both the CMU and SMU components which required heat sinking are mounted in such a manner as to have a direct heat path to the base mounting surface. Most of these components are only on for a short duration.

4.2 Shock and Vibration

The CMU is similar in configuration to the SSB/DSB Multiplexer (NASA Contract NAS8-21164). The difference in configuration is the larger size printed circuit boards and case used for the CMU. The printed circuit boards for CMU are grouped in pairs forming a module with two boards mounted back-to-back on a frame across the top with spacers mounted in between forming a box type construction.

The larger case is reinforced in the center by two web members. The larger size case will lower the resonant frequency and, this being a random vibration test only, will be a definite advantage. The SSB/DSB Multiplexer had to meet both sine and random vibration tests.

The operational shock test for this unit is a lesser requirement than for the SSB/DSB Multiplexer and with the design margin the non-operating shock will be tolerable.

The SMU is similar in design to a Peripheral Multiplexer Unit which was designed and tested at the Martin Marietta facility. This unit successfully passed a random vibration level of 67.5 g rms overall, with a maximum intensity of 4 g^2/Hz between 380 and 750 Hz. The g rms overall for the SMU is 23.9 with a maximum intensity of 0.6 g^2/Hz between 100 and 600 Hz.

4.3 Accelleration and Acoustic Susceptibility

The CMU is similar in design to the SSB/DSB Multiplexer and is designed to meet the same requirements for vibration. Therefore it is expected that with the acceleration and acoustical tests being at a lower level comparitively to the vibration levels there will not be any difficulty in meeting them. The SMU is a much smaller unit, has a low profile and is required to meet a higher random vibration level; therefore the above tests should not present any difficulty for this unit either.

82

4.4 Humidity, Corrosive Contaminants, Oxidation, and Shelf Life

For both the CMU and the SMU a sealed case provides protection for internal components. External components are protected by the proper finish.

4.5 Electromagnetic Interference

The design requirements of the solid state sequencer system are identified in the contract statement of work as follows:

> 3.2.2.8 Electromagnetic Interference - The equipment shall meet the requirements of NASA Specification IESD 19-3A.

In lieu of an actual test, we can establish with a good degree of confidence that the equipment will comply with all aspects of IESD 19-3A with little or no modification. The success of complying with EMI requirements is primarily dependent upon successful decoupling of the power supply from the power bus. This must be effective bidirectional decoupling with respect to both conducted and radiated interference. The solid state sequencer system uses a power supply with electrical and mechanical designs that have been successfully tested to several EMI specifications. A history of some of the equipment tested with similar power systems is as follows:

1. A Spacecraft Microminiature PAM Decommutator was successfully tested to IESD 19-3 under MSC contract NAS9-8301. A report of the test is presented in Martin Marietta report MCR-69-370, Test Report for Spacecraft Microminiature PAM Decommutator System.

2. A Microfilm Storage and Display unit was tested to MIL-I-2660 under MSC contract NAS9-8144. A report of the test is presented in Martin Marietta Report MCR-69-354, Ptototype Microfilm Storage and Display Test Report Electromagnetic Interference Test.

3. Perhaps the most severe test of a similar electronics system was performed on a PCM Telemetry Systems for Earth Resources Aircraft, contract NAS9-8146. The report covering this test is Martin Marietta report MCR-69-286, PCM Telemetry for Earth Resources Aircraft End Item Test Report.

4. Other equipment using similar power systems has been tested under various contracts to MIL-I-6181, MIL-STD-826, and MIL-STD-461.

SECTION 5

APPROVED PARTS LIST

CONTRACTOR APPROVED PARTS LIST
SOLID STATE SEQUENCER SYSTEM NASA CONTRACT NAS9-9334

ITEM NO.	NAME	TYPE	COMMERCIAL EQUIVALENT	VENDOR'S PART NUMBER	SPECIFICATION IDENTIFICATION	USED ON ASSEMBLY	QTY PER APPLICATION	APPLICATION* RESTRICTION	QUALIFICATION STATUS
1	Transistors	NPN SW	2N2221A	2N2221A	MOT. CAT. 1968	S4	218		Apollo, TX/255E
2		Unijunction	2N2422B	2N2422B	G.E.		38		Apollo (2N2420A)
3		PNP-SW	2N2907A	2N2907A	FSC CAT. 1969		46		Apollo, TX, JPL, GSFC
4		NPN-SW	2N3227	2N3227	MOT. CAT. 1968		3		To be determined
5		PNP-SW	2N3251	2N3251	FSC/MOT.		88		TX, Apollo, JPL, Martin
6		NPN-HiV	2N3499	2N3499	MOT. CAT. 1968		62		Apollo, Jan/366
7		NPN-SW	2N3507	2N3507	MOT.CAT. 1968		4		Antelope, IDEP Jan./349, Apollo
8		PNP-HiV	2N3635	2N3635	MOT. CAT. 1968		24		TX/357, Martin, IDEP
9		NPN DRIVER	MM3737	MM3737	MOT.		134		To be determined
10			2N4014	2N4014				As optional usage to MM3737	Optional Replacement for MM3737
11			2N3737	2N3737					
12		PNP DRIVER	2N3765	2N3765	MOT. CAT. 1968		59		To be determined
13		NPN-SW	2N3947	2N3947	MOT. CAT. 1968		121		Apollo, MSD, TO-27
14		PNP-HiV	2N4031	2N4031	FSC CAT. 1969		20		To be determined
15		NPN-PWR	2N4070	2N4070	SOL. CAT. 1968		8		To be determined
16		NPN-PWR	2N4071	2N4071	SOL. CAT. 1968		8		To be determined

ITEM	NAME	TYPE	COMMERCIAL EQUIVALENT	VENDOR'S PART NUMBER	SPECIFICATION IDENTIFICATION	USED ON ASSEMBLY	QTY PER APPLICATION	APPLICATION* RESTRICTION	QUALIFICATION STATUS
	Transistors					S4			
17		FET	2N4392	2N4392	UNION CARBIDE		1		To be determined
18		PNP-PWR	2N4398	2N4398	MOT. CAT. 1968		2		Same as 2N4399 Viking
19		NPN-HiV	2N4863	2N4863	SOL./PIRGO		8		To be determined
20		NPN Driver	2N4999	2N4999	FAIRCHILD		3		To be determined
21		PNP-PWR	2N5007	2N5007	FSC.CAT. 1969		8		To be determined
22		PNP-SW	2N5153	2N5153	FSC.CAT. 1969		3		Viking
23		PNP-HiV	2N5357	2N5357	MOT. CAT. 1968		8		To be determined
24		NPN-HiI	2N5579	2N5579	RCA		4		To be determined
25		NPN DUAL	2N2218A	MD2218A	Motorola		83		↓
26		PNP DUAL	MM4545	MM4545	Motorola		8	As optional usage to 2N5357	
27		NPN-HiI	SDT8602	SDT8602	SOL. CAT. 1968		4		To be determined
28	Diode	Hi. Cond.	IN645	In645	T.I. CAT. 1968		33		Apollo, TX, GSFC, MSD
29		Zener	IN746A	IN746A	T.I. CAT. MOT		11		Apollo, TX, JPL
30		Zener	IN748A	IN748A	Motorola		3		Apollo, TX, JPL
31		Zener	IN750A	IN750A	Motorola		2		Apollo, TX, JPL
32		Zener	IN752A	IN752A	T.I. INT. MOT		1		↓
33		Zener	IN756A	IN756A	T.I. INT. MOT		4		
34		Zener	IN827	IN827	MOT. CAT. 1968		1		Apollo, TX, GSFC, MSFC, JPL, NAR-S10, ATM

ITEM	NAME	TYPE	COMMERCIAL EQUIVALENT	VENDOR'S PART NUMBER	SPECIFICATION IDENTIFICATION	USED ON ASSEMBLY	QTY PER APPLICATION	APPLICATION* RESTRICTION	QUALIFICATION STATUS
35	Diode	Zener	IN961B	IN961B	MOT. INT.	S4	5		
36		Zener	IN963B	IN963B	MOT. INT.		36		
37		Zener	IN965B	IN965B	MOT. INT.		12		
38		Zener	IN967B	IN967B	MOT. INT.		20		
39		Signal	IN4148	IN4148	G.E.		225		TX/116,IDEP
40		Hi COND.	IN4608	IN4608	G.E.		753		To be determined
41		Hi COND.	IN4942	IN4942	UNITRODE		20		TX, GSFC, IDEP
42		Hi Speed	UTX 215	UTX 215	UNITRODE		14		By similarity to UTX210-JPL
43		Hi Speed	UTX 4110	UTX 4110			5		MSD, TO27, IDEP
44		Zener	UZ7720R	UZ7720R			2		To be determined
45		Zener	UZ7827	UZ7827			4		To be determined
46	Diode	Zener	UZ7850	UZ7850	UNITRODE		19		To be determined
47	Resistor	0.1W,1% Metal Film		MS4C	ELECTRA		84		To be determined
48		1/8W,1% Met. Film	MF5C	MF5C	ELECTRA		1711		Martin Std., Apollo, Similar to MIL-R-10509 & MIL-R-55182
49		1/2 W,1% Met. Film	MEB-T-0	MEB-T-0	IRC		34		Similar to MIL-R-10509, MIL-R-55182
50		1/2 W, 1% WW	AS-1/2	AS-1/2	IRC		139		By similarity to AS-1, AS-2 (Apollo)
51		1 W, 1% WW	AS-1	AS-1	IRC		122		Apollo, OCS

ITEM	NAME	TYPE.	COMMERCIAL EQUIVALENT	VENDOR'S PART NUMBER	SPECIFICATION IDENTIFICATION	USED ON ASSEMBLY	QTY PER APPLICATION	APPLICATION* RESTRICTION	QUALIFICATION STATUS
52	Resistor	2W, 1% WW	RS-2A	RS-2A	DALE CAT. A	S4	10		Meets MIL-R-26C and MIL-R23379
53		5W, 1% Wirewound		RH-5	DALE		16		To be determined
54		5W, 1% WW	RS-5	RS-5	DALE CAT. A		8		MIL-R-39007
55		10W, 1% Wirewound		G10	DALE		2		To be determined
56		10W, 1%, WW	RH-10	RH-10	DALE CAT. A		4		By similarity to NH10 Apollo, RE65
57		25 W,1% WW	RH-25	RH-25	DALE CAT. A		8		Apollo, RE-70
58		1/8 W, 1% Met. Film	MFF-1/8 TI	MFF-1/8 TI	DALE CAT. A			(SEE MF5C AS OPTIONAL USAGE TO MF5C	IDEP
59	Capacitor	Metallized Polycarbonate X483	X483	X483	TRW		14		To be determined
60		Tantalum	150D	150D	SPRAGUE		159		Apollo, MSD, OCS, JPL
61		Tantalum	A Series	A Series	KEMET			AS OPTIONAL USAGE TO 150D	Apollo, MSD, TO27, Polaris, IDEP
62		Tantalum	J Series	J Series	KEMET			AS OPTIONAL USAGE TO 150D	Apollo, MSD, TO27, Polaris, IDEP
63		Ceramic	K Series	K Series	KEMET		102		TARTAR, TERRIER, IDEP, MIL-R-39003, Apollo
64		Ceramic	VK 30	VK30	Vitramon C-10C		44		Apollo, TERRIER, IDEP, Marriner, MOD III

ITEM	NAME	TYPE	COMMERCIAL EQUIVALENT	VENDOR'S PART NUMBER	SPECIFICATION IDENTIFICATION	USED ON ASSEMBLY	QTY PER APPLICATION	APPLICATION RESTRICTION	*QUALIFICATION STATUS
65	Capacitors	Ceramic	CK18BX	CK18BX	SAN FERNANDO	S4	578		To be determined
66		Ceramic	CK18DX	CK18DX	SAN FERNANDO		38		
67		Ceramic		C102-1502-KS	I.C.C.		3		
68		Ceramic		C20C-	VSCC		121		
69		Ceramic		C062-	KEMET		59		
70		FEED-THRU		1250-003	ERIE		18		
71	Capacitor	Ceramic		CK06BX104	KEMET		1		
72	Filter			2120-013	USCC		2		To be determined
73	Core	Tapewound	80529-1/2 D-MA	80529-1/2D-MA	MAGNETICS TWC300		176		Similarity to M Std. 80530
74		Tapewound	80521-1/8 D-MA	80521-1/8 D-MA	MAGNETICS TWC 300		309		(Similarity to M Std. 80530)
75		Ferrite	1041T060-3E2A		FERROXCUBE 33B		371		Martin Standard
76		Ferrite	846T250-3E2A				2		Martin Standard
77		Powered Molly		55121-A2	MAGNETICS INC.		4		To be determined
78		Powered Molly		55051-A2	MAGNETICS INC.		1		To be determined
79	Integrated Circuit	TTL	SN5400		T.I.		102		(Similar to M Standard 55926) NASA-MSFC B5M03766
80		TTL	SN5401		T.I.		4		(Similarity-Same die as 5400)
81			SN5402				119		(Similarity-Same die)

ITEM	NAME	TYPE	COMMERCIAL EQUIVALENT	VENDOR'S PART NUMBER	SPECIFICATION IDENTIFICATION	USED ON ASSEMBLY	QTY PER APPLICATION	APPLICATION* RESTRICTION	QUALIFICATION STATUS
82	Integrated Circuit	TTL	SN5410		T.I.	S4	37		NASA-MSFC-85M03766 IDEP
83			SN5420				7		
84			SN5430				12		
85			SN5440				36		
86			SN5450	SN5450			32		NASA-MSFC-85M03766 IDEP
87			SN5472				4		
88			SN5473				22		
89			SN5474				61		
90			SN5482	SN5482			15		
91			SN5486	SN5486			40		
92			SN54121	SN54121			36		
93			SN54L00				13		
94			SN54L20				2		
95			SN54L30				5		
96			SN54L73				9		
97	Integrated Circuit	TTL	SN54L74		T.I.		10		NASA-MSFC-85M03766
98		Linear	LM101	LM101	Data Sheet Jan. 1968		10		Apollo, IDEP, NASA-MSFC, Viking
99		Linear	LM103	LM103	National Sem.		7		To be determined
100		Linear		MC1711F	MOTOROLA		13		

ITEM	NAME	TYPE	COMMERCIAL EQUIVALENT	VENDOR'S PART NUMBER	SPECIFICATION IDENTIFICATION	USED ON ASSEMBLY	QTY PER APPLICATION	APPLICATION* RESTRICTION	QUALIFICATION STATUS
101	Crystal	8 MHz	KTO69-30	KTO69-30	MONITOR	S4	1		To be determined
102	Memory Stack	1024 x 12			EMI		1		
103	Transformer Bobbin	Nylon	SN1226-2		COSMO PLASTIC CO.		4		
104	Fuse Resistor	Fast Blow		F 166	RCL CAT. 689		66		
105	↓	1 OHM Controlled Blow		F 167-1	RCL CAT. 689		43		To be determined
106	Fuse Resistor	0.25 OHM Controlled Blow		F 167-1/4	RCL CAT. 689		6		To be determined
107	Fuse	Fast Blow		273 Series	LITTLEFUSE CAT. 15-A		2		To be determined
108	Fuse Holder			2820028	LITTLEFUSE		2		
109	SCR	MED. I	2N684	2N684	G. E. MOT.		56		
110	SCR	LOW I	2N2325A	2N2325A	G. E. MOT.		56		
111	SCR	MED I	2N3655	2N3655	GE		1		To be determined
112	Diode	Zener	IN968B	IN968B	MOT. INT.		1		Tx, GSFC, MSFC, JPL, NAR-SID, ATM
113	Conversion Pad	Transistor Mounting		7717-	THERMALLOY		788		To be determined

ITEM	NAME	TYPE	COMMERCIAL EQUIVALENT	VENDOR'S PART NUMBER	SPECIFICATION IDENTIFICATION	USED ON ASSEMBLY	QTY PER APPLICATION	APPLICATION* RESTRICTION	QUALIFICATION STATUS
114	Solder Terminal	Insulated		1980-XB094	CAMBION	S4	24		To be determined
115		Turret		2043-2	CAMBION		603		
116		Turret		2085-2	CAMBION		135		
117	Connector	PC Board		UPC2B	BURNDY		28		
118		PC Board		UPC3B	BURNDY		44		
119		Test Point		AMP 203976	AMP		39		
120		Case Internal		DDMA-	CANNON		4		
121		Case Internal		DDM-	CANNON		2		
122		Case External		UR24-	DEUTSCH		3		
123		Case External		MD53-	MICRO-DOT		6		
124	Transistor	NPN-PWR.	2N5002	2N5002	FSC CAT. 1969		2		Same chip & Pkg. as 2N5004 Viking

6. ACCEPTANCE TEST RESULTS

Temperature testing was done with the technical monitor, Gary Johnson, present. Successful functional tests were conducted with the temperature initially set at +160°F and then at -0°F. In addition, operation was checked while the temperature was changing from room temperature to +160°F and from +160°F to -0°F. The only problem encountered during this test was that the system continued past STOP commands in instances where the STOP command occurred after a time count had been interrupted. This was agreed to be a non-temperature dependent problem, and was subsequently fixed by increasing the number of clear turns on the ONEs generator CTL or CTL Board No. 7. These tests were not repeated for Martin Q.C., since Mr. Johnson proclaimed himself satisfied.

The SMJC was tested at room temperature, -25°F, and +200°F in accordance with Section 6.0 of the acceptance test procedure and operated satisfactorily.

Copies of the results of full load testing and voltage range testing will be delivered with the system.

7. CONFORMANCE WITH STATEMENT OF WORK

7.1 General

This section details how the system meets the design goals and specifications set forth in Exhibit A of the Statement of Work and not covered elsewhere in this report.

7.2 Weight, Volume, Power Consumption

The system weight is 104 lbs. for two parallel channels. This exceeds the design goal of 80 lbs.

The system volume has been calculated at 2,890 cu. in. which is slightly below the design goal of 3,000 cu. in. for two parallel channels.

The power consumption for a two channel, based on a logic bus voltage of +28 VDC, is about 10 watts as opposed to the design goal of 36 watts.

7.3 Growth Factor

The sequencer is required to exhibit the capability of ten percent growth over the functions presently specified. To meet this requirement, the following steps have been taken:

A. Ten percent input filter circuit spares have been left on CTL Boards 1 and 6.

B. Event Logic Block 1 has been implemented to accept 13 inputs while only 11 are presently used (see CTL Board No. 3).

C. Event Logic Block 2 has been implemented to accept 8 inputs, while only 7 are used (see CTL Boards 2 and 5).

D. The memory has 20 percent unused capacity.

E. The six output switch boards have 23 percent unused capacity.

F. The six PFC boards have 8.3 percent unused capacity.

G. The output switch base plate has 10 percent unused capacity.

H. When items E, F, and G are taken together, an unused output capacity of about 12 percent is available.